Set-27.

(135)

Unit-I

Unit-I PN Junction Devices

PN Junction Diode - Structure, operation & VI characteristics, diffusion & transient capacitance - Rectifiers - Half Wave & full Wave Rectifier - Display Devices - LED, Laser diodes, Zener Diode - characteristics - Zener Reverse characteristics - Zener as regulator.

PN Junction Diode:

Semiconductors:

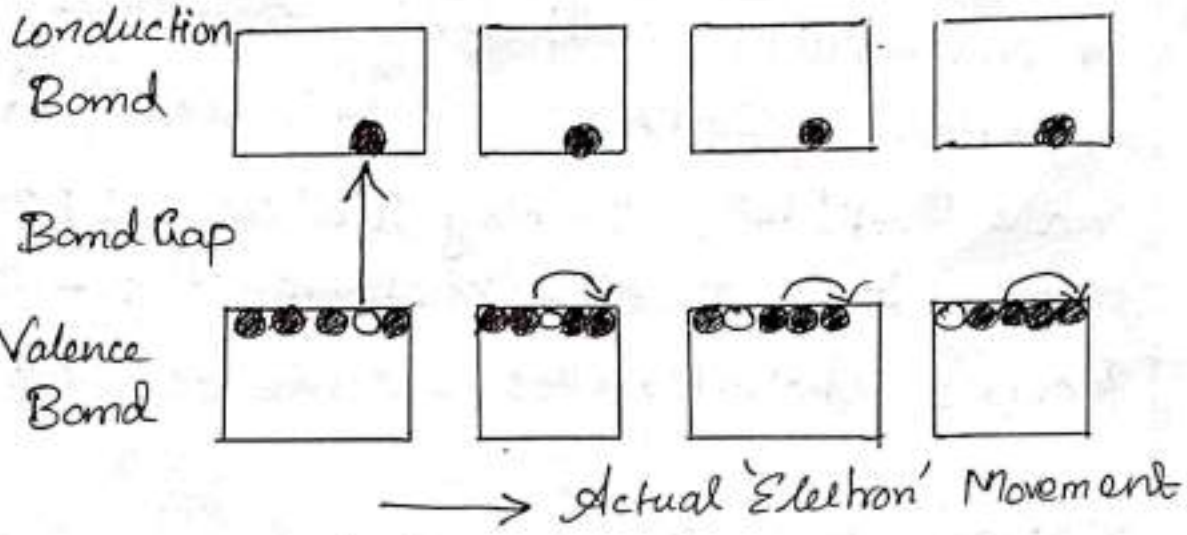
A Semi conductor is a substance which has resistivity 10^{-4} to 0.05Ω in between conductor & insulator.

Example: Germanium, Silicon, Selenium

The energy gap between conduction band & valance band is very small ≈ 1eV

Therefore smaller electric field is required for conduction bank low temperature. The Valence band of the

Semiconductor is completly full and condution band is empty. If the temperature is increased more valence electrons cross over to the condution band the conductivity increases.



The electrical conductivity of Semiconductor is in the range of 10^{-3} to 10^{-6} Ω/cm.

Types of Semicoductor:

(i) Intrinsic Semiconductors
(ii) Extrinsic Semiconductors

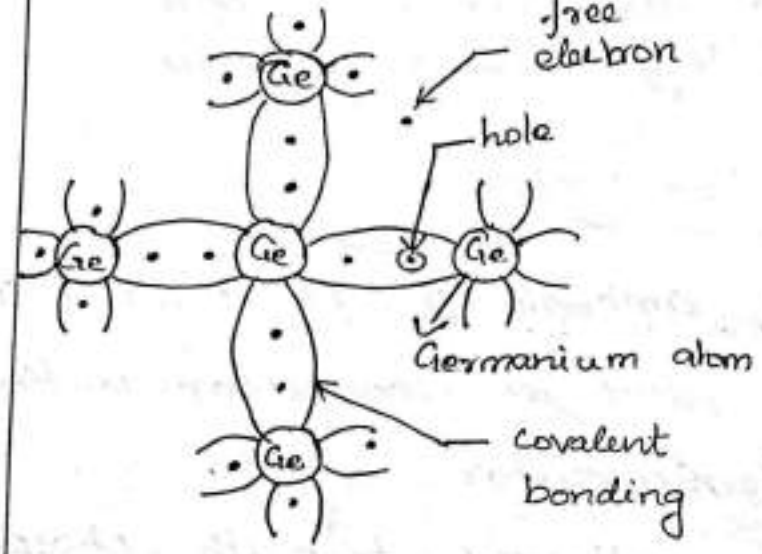
Intrinsic Semiconductors:

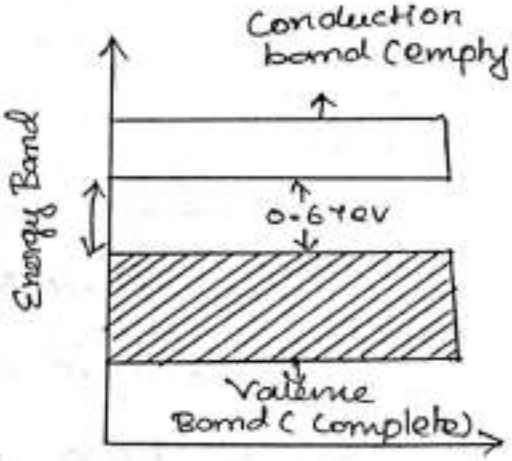
A Semiconductor which is in the extremely pure form is known as an intrinsic Semiconductor. The Hole - electron pairs

are created even at room temperature also. There being as many holes as the free electrons.

If potential difference is applied across intrinsic semiconductor, the electrons will move towards the positive terminal while the holes will drift towards the negative terminal.

The temperature of the semiconductor increase, the no. of hole - electron pairs increase. The total current inside the semiconductor is the sum of currents due to free electrons & holes.





Extrinsic Semiconductor:

The conductivity can be increased by the addition of a small amount of suitable

metallic impurity. It is also known as impurity Semiconductor.

The process of adding impurity atoms to the intrinsic Semiconductor is called doping. The purpose of adding impurity is to increase either the no. of free electrons or holes in a Semiconductor.

Impurity atoms containing five valence electrons is called pentavalent impurity atoms & the impurity atoms containing three Valence electrons is called trivalent impurity atoms. Types are,

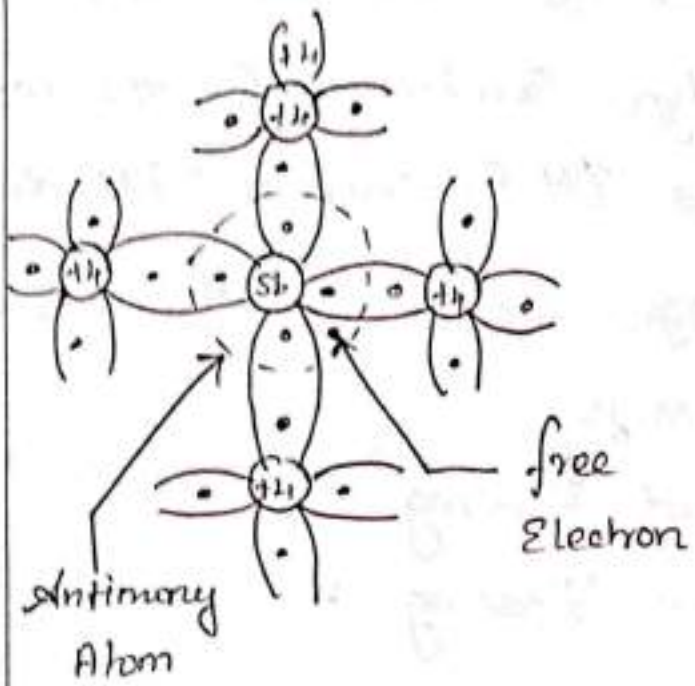
→ N Type Semiconductor
→ P Type Semiconductor

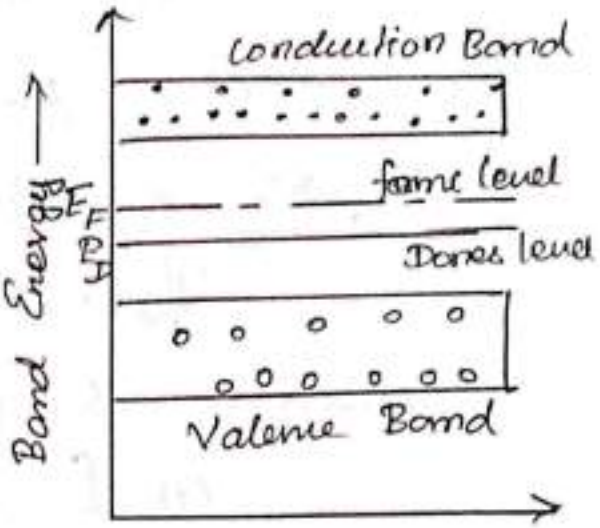
N - Type Semiconductor:

A small amount of pentavalent impurity is added to a pure Semiconductor is known as N- type Semiconductor.

Arsenic, antimony, bismuth, phosphorus. elements donate excess electron carriers. The structure of a Silicon crystal lattice containing as antimony atom at the central

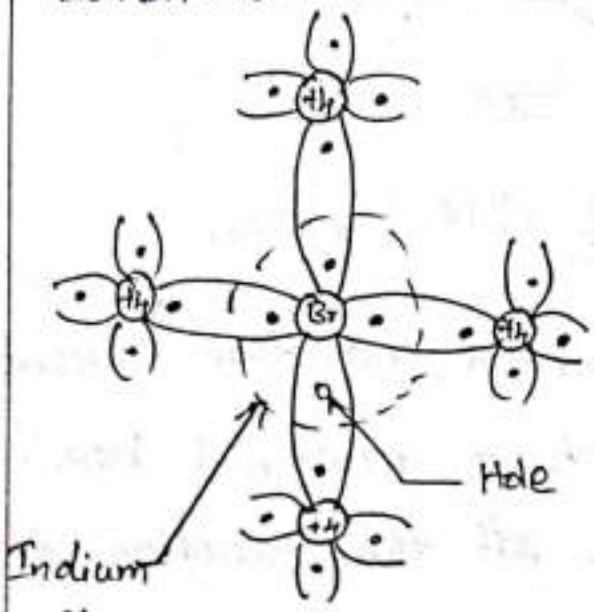
Position.

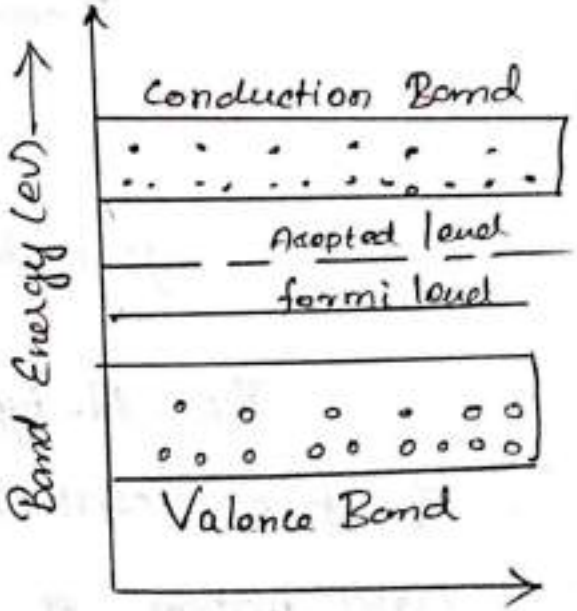




P- Type Semiconductor:

A small amount of trivalent impurities is added to a pure semiconductor is known as P-type Semiconductor. Ex, Gallium(Ga), Boron(B).



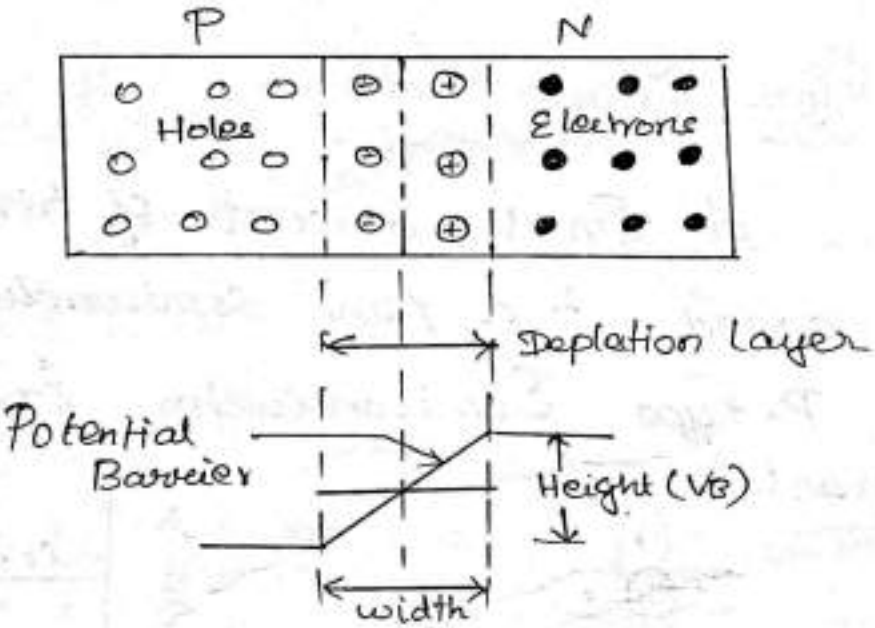


PN Junction Diode:

When a P-type Semiconductor is joined to a N-type Semiconductor the contact surface is called PN Junction (or) PN diode.

The voltage across PN Junction can be applied in two ways.

(i) forward Biasing
(ii) Reverse Biasing



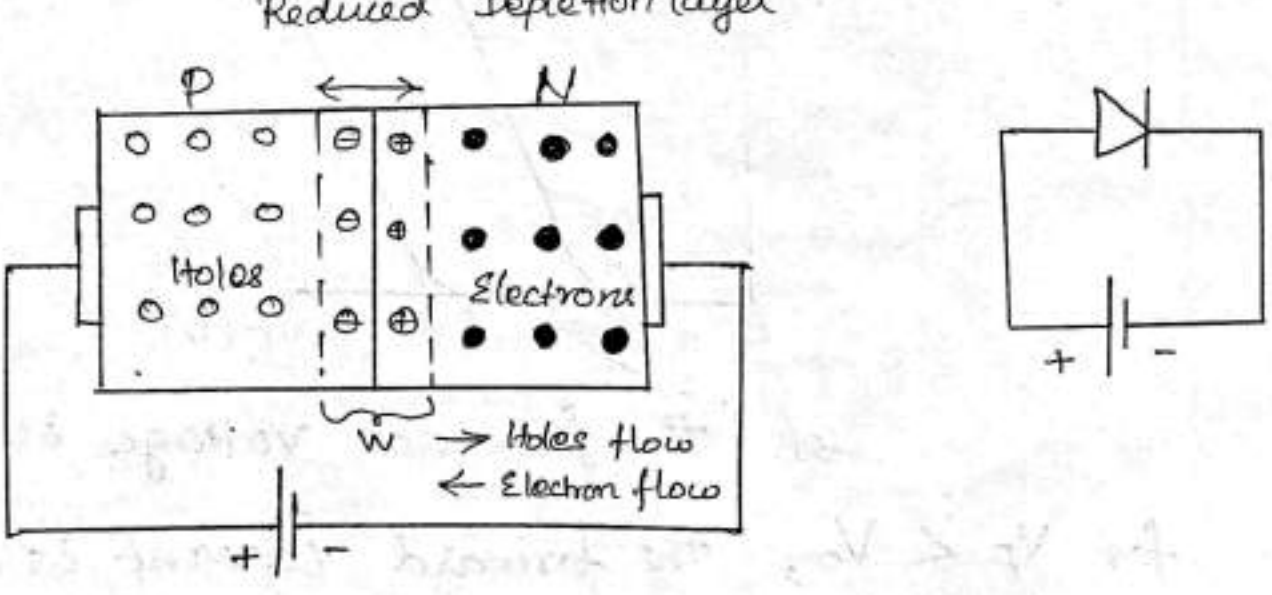
formation of PN Junction

The N-type material has High concentration of free electrons & P type material has high concentration of holes. At the junction, there is a tendency to free the N-type electrons diffus

Over the P-type holes from the P-side to the N-Side. This process is called diffusion. Thus a barrier is set up against further movement of charge carriers (holes & free electrons). This is called potential Barrier or Junction barrier (V_B). The potential Barrier is of the order of 0.1V to 0.3V. The mobile charges have been depleted in this region. It is known as depletion layer.

Forward Bias:

In this case positive Terminal of the Voltage source is connected to the P-side & negative terminal to the N-Side as shown in the fig.

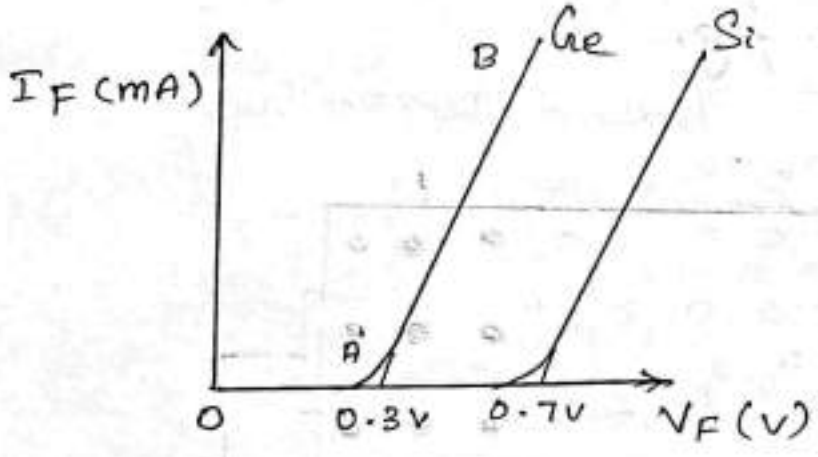


a large amount of current flows through the junction under this condition.

Under forward Bias condition, the applied Positive potential repels the holes in P-type region so that the holes move towards the junction. The applied negative potential repeal the Electrons in the N-type region & the electron moves towards the junction eventually; if applied Potential is more than the internal barrier Potential the depletion region & internal barrier potential disappear.

Characteristics of forward Bias:

The V-I characteristics of a PN Junction Diode is shown.

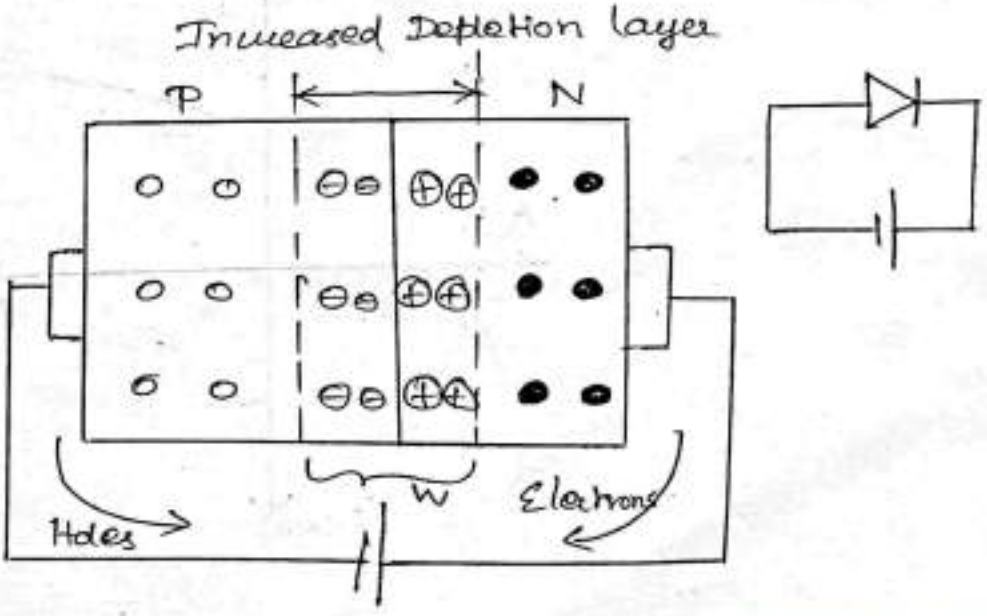


As the forward voltage is increased for $V_F < V_0$, the forward current is almost

zero, because the potential Barrier prevents the holes from P-region & electron from N-region to flow across the depletion region in the opposite direction. for $V_F > V_0$ the potential Barrier at the junction completely disappears & hence the holes cross the junction from P-type to N-type & electrons across the junction in the opposite direction.

Reverse Bias:

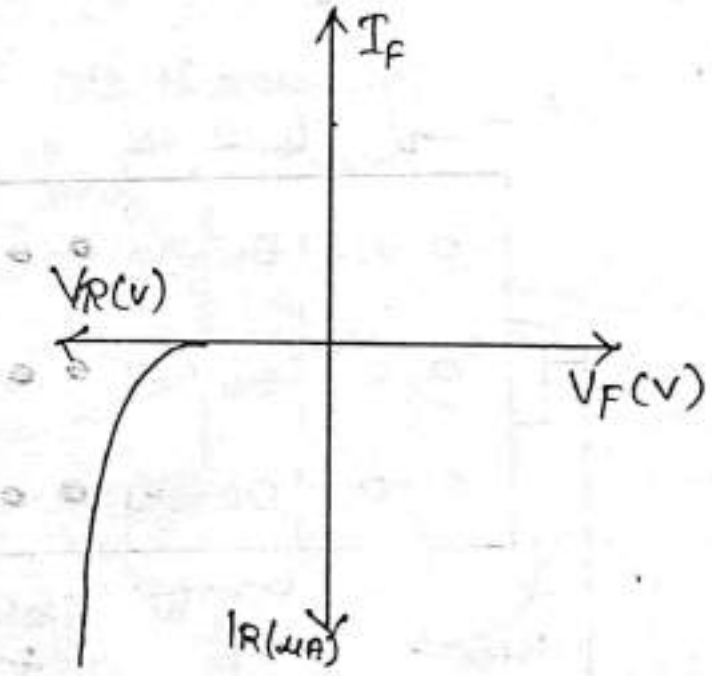
In this case, positive terminal of the voltage source is connected to the N-side & Negative terminal to the P-side as shown in the fig. No current flow through junction.



Under Reverse Bias condition holes from the majority carriers of the P-Side move towards the negative terminal of the battery & electrons which form the majority carriers of the N-Side are attracted towards the positive terminal of the battery. The width of the depletion region which is deflected by mobile charge carriers increases.

Characteristics of Reverse Bias:

At the reverse Bias the Barrier Voltage of the diode is increased. Therefore the diode resistance becomes very high.

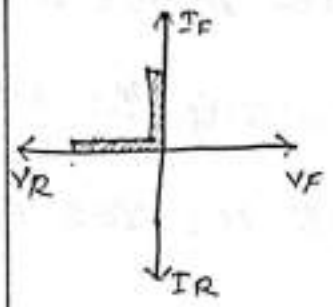


In practice a very small current in the range of micro amperes flows in the circuit with the reverse Bias. This is known as reverse current & is due to the minority carriers. As we are increasing the reverse voltage, there may be a small increase in current.

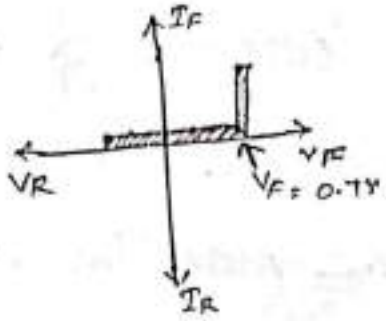
At a particular voltage, we are getting a certain rise in the curve. This voltage is known as breakdown voltage. At this Particular voltage the minority carrier get enough kinetic energy to break the junction. As a result, the junction is destroyed & diode allows the current.

VI characteristics:

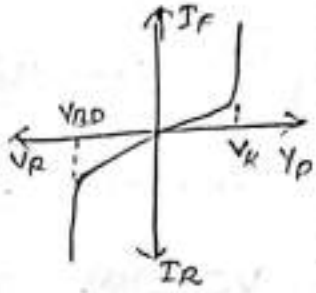
Ideal Diode



Practical diode



Complete-diode mod



Knee Voltage (V_K)

The voltage at which device current suddenly increases or decreases.

Breakdown Voltage (V_{BO})

The reverse voltage at which the junction break down occurs.

Limiting Values of PN Junction Diode:

The PN junction operates satisfactorily within certain limiting values.

i) Maximum forward current:

It is the highest instantaneous current under forward bias condition that can flow through the junction.

ii) Peak Inverse Voltage (PIV):

It is the maximum reverse voltage

that can be applied to the PN Junction.

iii) Maximum Power Rating:

It is the maximum power that can be applied to the PN dessipated at the junction without damaging the junction.

Power dessipation is the product of voltage across the junction & current through the junction.

Diode current equation:

The diode current equation relating the voltage V & current I is given by

$$I = I_o \left[e^{(V/\eta V_T)} - 1 \right]$$

where I : diode current

I_o : diode reverse saturation current at room temperature

V : external voltage applied to the diode

η : a constant, 1 for Ge & 2 for Si.

$V_T = \frac{KT}{q} = \frac{T}{11,600}$, thermal voltage

where K : Boltzmann's constant (1.38×10^{-23} J/K)

q : charge of the electron (1.6×10^{-19} C)

T : temperature of the diode junction (°K)

At room temperature (T = 300°K), V_T = 26 mV.

Diffusion & Transient Capacitance:

Transition (OR Space charge) Capacitance:

An applied reverse bias causes the majority carriers to move away from the junction, thereby uncovering the immobile charges. If this reverse voltage is increased, the thickness of the space-charge region at the junction increases.

This further increases the number of uncovered charge & results a capacitive effect. This effect is defined by an incremental capacitance, C_T given by.

This capacitance which is due to depletion layer is known as depletion capacitance or transition capacitance can be expressed as

$$C_T = \frac{dQ}{dV}$$

where,

dQ is the increase in charge caused by a charge dV in voltage.

A charge of voltage dV in a time dt will result in a current $i = dQ/dt$. Hence,

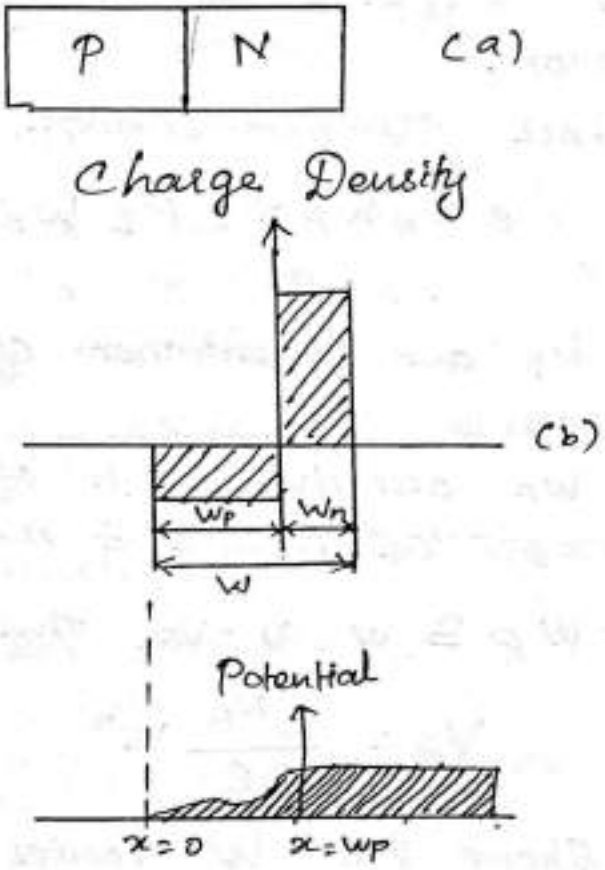
$$i = C_T \frac{dV}{dt}$$

It shows that C_T is not a constant, but

depends upon the magnitude of the reverse voltage, Hence, C_T is defined with respect to a charge & voltage.

$$C_T = Q/V$$

Case i : for an Alloy / fusion / step Graded junction



An alloy junction is one in which there is an abrupt change from acceptor ions on one side to donor ions on the other side. Such a condition is formed by placing indium, which is trivalent in nature, against an N-type impurity doped germanium & heating the combination to a hight temperature for a short time.

Some of the indium will dissolve into the germanium to change the germanium from N to P type at the junction.

Consider the charge density as a function of distance from the alloy junction.

Assume that the acceptor ion impurity density is much smaller than the donor impurity concentration.

Since the net charge must be zero,

$$eN_A W_p = eN_D W_n$$

where

N_A & N_D are concentration of the acceptor & donor ions.

W_p & W_n are the width of the depletion regions on the p-side & n-side respectively.

At $x = W_p \cong W$, $V = V_B$, thus

$$V_B = \frac{eN_A}{2\varepsilon} W^2$$

It shows that W varies as $V_B^{1/2}$.

Consider that V is the applied bias & V_0 is the contact potential, then $V_B = V_0 - V$. If the area of the junction is A, the charge with distance w is given by,

$$Q = eN_A W_A$$

We know,

$$C_T = \left| \frac{dQ}{dV} \right| = eN_A A \left| \frac{dW}{dV} \right|$$

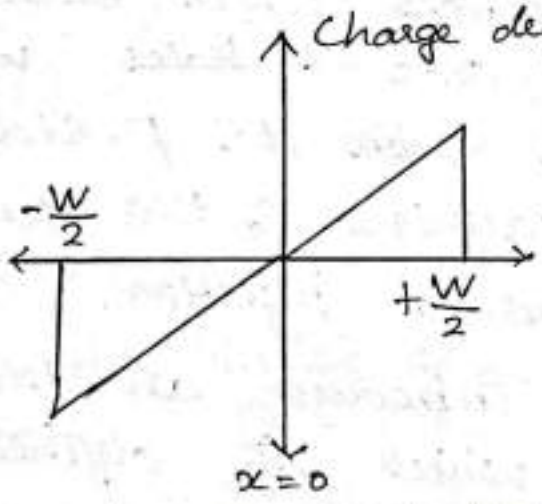
Hence $\frac{dW}{dV} = \frac{\varepsilon}{eN_A W}$ & $C_T = \frac{\varepsilon A}{W}$

It represents the expression obtained for a parallel-plate capacitor of area A & plate separation W containing a material of permittivity ε.

Case 2: for a Grown/Linearly Graded junction:

It is obtained by a drawing a single crystal from a metal of germanium whose type is changed during the drawing process by adding first P type & then N-type impurities. for such a junction, the charge density varies gradually across the junction.

If $N_A < N_D$, then $W_p \gg W_n$, Neglect W_n & assume that the entire barrier potential V_B appears across the P-side or across the uncovered acceptor ions.



The relation between potential & charge density is given by the poison's equation,.

$$\frac{d^2V}{dx^2} = \frac{e N_A}{\varepsilon}$$

where,

ε is the permittivity of the Semiconductor.

Integrating the above equation.

we get,

$$V = \frac{e N_A x^2}{2\varepsilon}$$

for this function, if an analysis is carried out, we find that $C_T = \varepsilon A/W$ & W varies as $V_B^{Y_2}$

Diffusion (or Storage) capacitance:

If the diode is biased in the forward direction, the potential barrier at the junction is lowered & diffusion of charge take place. Hence the electrons which enter the P side from the N-side & holes which enter the n-side from the P-side constitute minority carriers & this process is called minority carrier injection.

Hence, we introduce an incremental capacitance which is defined as the rate of change of injected charge with applied voltage. This capacitance is called diffusion or storage capacitance C_D.

Assume that one side of the diode, say the P-side is early doped, so that the current I is carried entirely by holes moving from the P-side to the n-side or $I = I_{pn}(0)$.

The excess minority charge Q will then exist only on the n-side & is given by,

$$Q = \int_0^\infty A e P_n(0)\, e^{-x/L_p}\, dx.$$

$$C_D = \frac{dQ}{dV} = A e \frac{dP_n(0)}{dV} L_p.$$

The hole current I is given by,

$$I_{pn}(x) = \frac{A e D_p P_n(0)}{L_p}\, e^{-x/L_p}$$

with $x = 0$

$$I_{pn}(x) = I = \frac{A e D_p P_n(0)}{L_p}$$

$$\therefore \frac{dP_n(0)}{dV} = \frac{L_p}{A e D_p} \cdot \frac{dI}{dV} = \frac{L_p}{A e D_p} g.$$

where,

$g = dI/dV$ = diode conductance.

$$C_D = A e L_p \frac{L_p}{A e D_p} g = \frac{L_p^2 g}{D_p}.$$

we know, mean lifetime for holes, $\tau_p = \tau$ & is given by,

$$\tau = \frac{L_p^2}{D_p}.$$

Then $\therefore C_D = Ig$

Diode resistance. $r = \frac{\eta V_T}{I}$ ——— (A) $\therefore g = \frac{I}{\eta V_T}$ ——— (B)

Substituting equations.

The diffusion capacitance.

$$\boxed{C_D = \frac{II}{\eta V_T}} \quad \text{——— (C)}$$

The expression (C) is only for hole movement. Similarly, we can derive an expression for C_D electron movement.

The sum of C_{Dp} & C_{Dn} given the total diffusion capacitance C_D.

for a reverse bias C_D may be neglected compared to C_T, Similarly for a forward bias, C_D is usually much larger than C_T,

also $r C_D = \tau$.

where,

$r C_D$ is the diode time constant & it equals the mean lifetime of minority carriers which lies in the range of nanoseconds to hundreds of microseconds.

(11)

Rectifiers

A circuit that converts ac to pulsating dc.

Types:

1, Half wave rectifier
2, full-wave rectifier
3, Bridge rectifier

Half-wave rectifier:

→ Half wave rectifier is simply a diode that is placed in series between a transformer (or ac line input) & its load.

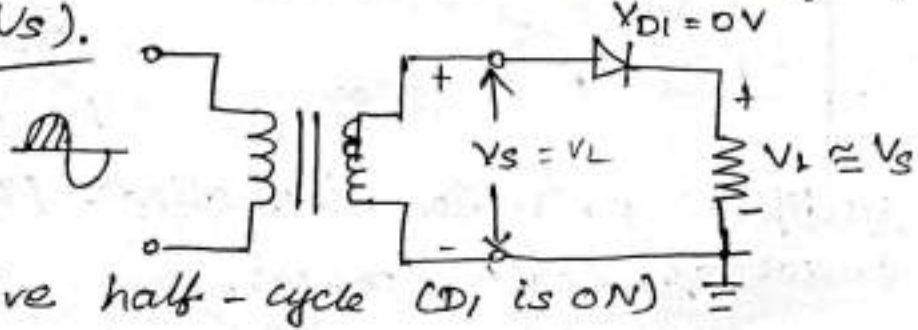
→ It eliminates either the negative or positive alternation of the input.

→ As it requires less no. of parts, it is cheapest of all.

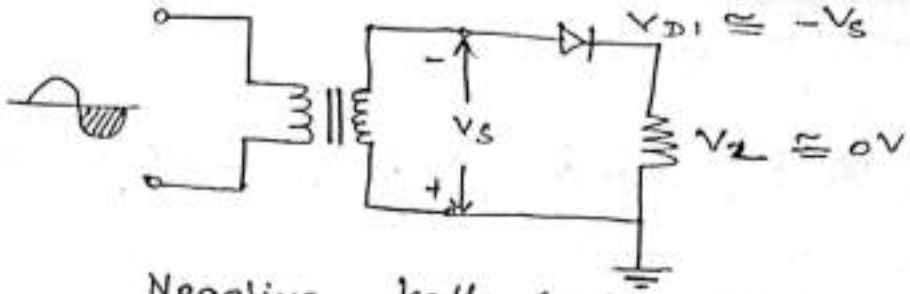
Positive Half-wave rectifier:

→ During the positive half-cycle of the input, D1 is forward biased & provides a path for current.

→ This allows a voltage V_L across R_L to be developed which is approximately equal to the voltage across the secondary of the transformer (V_S).



Positive half-cycle (D1 is ON)



Negative half-cycle (D_1 is OFF)

→ D_1 is reverse-biased, preventing conduction in the circuit when the polarity of the input reverses.

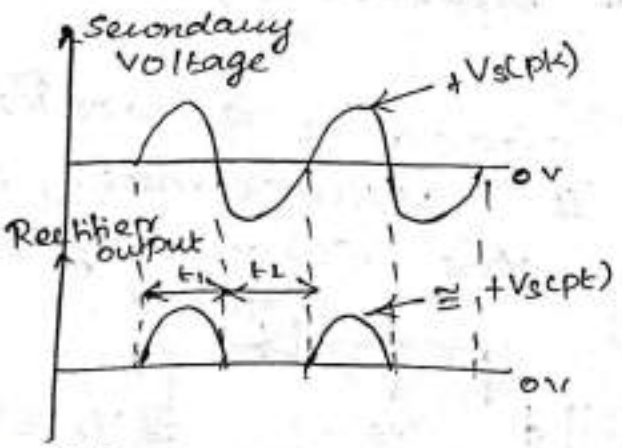
→ Since no current flows through R_L, the voltage across it is zero & across diode is approximately V_s.

Forward operation (closed switch) : $V_L \cong V_s$

Reverse operation (open switch) : $V_{D1} \simeq V_s$

Diode condition	V_{D1} (ideal)	V_L (ideal)
forward biased	0V	Equal to V_s
Reverse biased	Equal to V_s	0V

Ideal input & output waveforms:



→ During t_1, the diode is forward Bias & $V_L \cong V_s$

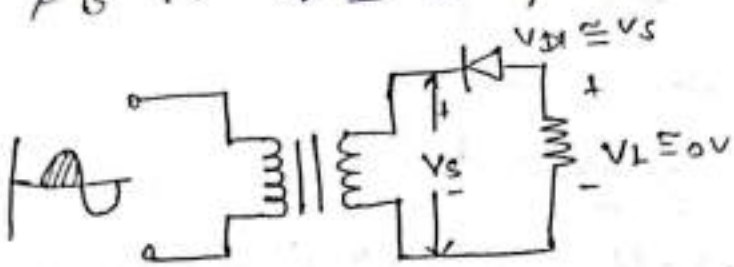
→ During t_2 the diode is Reverse bias & dp drops to 0V

→ The o/p from a Positive half-wave rectifier or when the diode points R_L is a series of positive pulses.

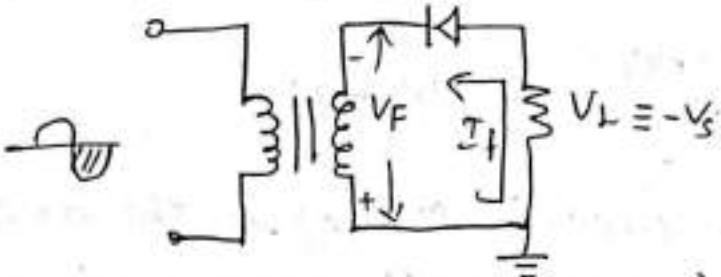
Negative Half-wave Rectifier

→ During the positive half-cycle of the input D_1 is R.B so $V_{D1} \cong V_s$ & $V_L = 0V$.

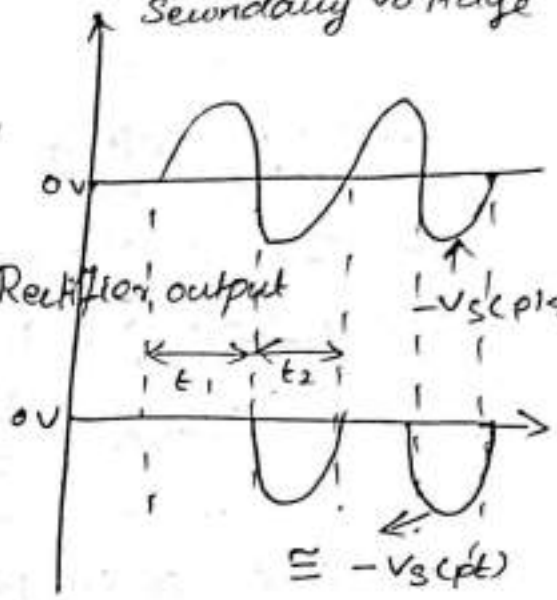
→ During the negative half-cycle of the input, D_1 is F.B ∴ $V_L \cong V_s$ & $V_{D1} = 0V$.



Positive half-cycle (D_1 is OFF)



Negative half-cycle (D_1 is ON)



→ The output from a negative half-wave rectifier or when the diode points towards the source is a series of negative pulses.

Load Voltage & Load current:

→ The peak load voltage is $V_{L(pk)} = V_{s(pk)} - V_F$

where V_F = diode forward voltage

$V_{s(pk)}$: peak secondary voltage of the transformer.

$$V_{s(pk)} = \frac{N_s}{N_p} V_{p(pk)}$$

where $\frac{N_s}{N_p}$: turns ratio of the transformer

$V_{p(pk)}$: the peak transformer primary voltage.

$$V_{P(PK)} = \frac{V_{rms}}{0.707}$$

The peak load current is

$$I_{L(PK)} = \frac{V_{L(PK)}}{R_L}$$

Average voltage & current:

→ The average voltage (V_{ave}) is the dc content of the voltage across the load.

$$V_{ave} = \frac{V_{(PK)}}{\pi} = 0.318\, V_{(PK)}$$

→ The average current (I_{ave}) is the d.c equivalent of an alternating current, measured with dc ammeter.

$$I_{ave} = \frac{V_{ave}}{R_L} = \frac{I_{PK}}{\pi} = 0.318\, I_{PK}$$

Peak Inverse Voltage (PIV):

→ The maximum reverse bias that will be applied to a diode in a given circuit is called the peak inverse voltage or PIV.

for HWR $PIV = V_{S(PK)}$

→ PIV is used to determine the minimum allowable value of V_{RRM} (Peak reverse voltage) for any diode used in the circuit

Ripple factor:

The ratio of rms value of a.c component to the d.c component in the output.

$$\gamma = \frac{V_{a.c\,rms}}{V_{d.c}} = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1}$$

$$\gamma = \sqrt{\left(\frac{V/2}{V/\pi}\right)^2 - 1} = \sqrt{\left(\frac{\pi}{2}\right)^2 - 1}$$

$$\boxed{\gamma = 1.21}$$

The amount of a.c present in the output is 121% of the d.c voltage, so HWR is not useful for converting a.c into d.c.

Efficiency:

The ratio of d.c output power to a.c input power is known as rectifier efficiency.

$$\eta = \frac{P_{d.c}}{P_{a.c}}$$

$$\eta = \frac{(V_{dc})^2/R_L}{(V_{rms})^2/R_L} = \frac{(V_{s(max)}/\pi)^2}{((V_{s(max)})/2)^2} = \frac{4}{\pi^2} = 0.406$$

$$\boxed{\eta = 40.6\%}$$

∴ The max efficiency of HWR is 40.6%.

Form factor:

$$\text{form factor} = \frac{\text{rms values}}{\text{average values}} = \frac{V_m/2}{V_m/\pi}$$

$$\boxed{ff = 1.57}$$

Peak factor:

$$P.f = \frac{\text{peak value}}{\text{rms value}} = \frac{V_m}{V_m/2} = 2$$

Transformer utilization factor: (TUF)

$$TUF = \frac{\text{dc power delivered to the load}}{\text{ac rating of the transformer secondary}}$$

$$TUF = \frac{I_m^2}{\pi^2} \cdot R_L \Big/ \frac{V_m}{\sqrt{2}} \cdot \frac{I_m}{2} = 0.287$$

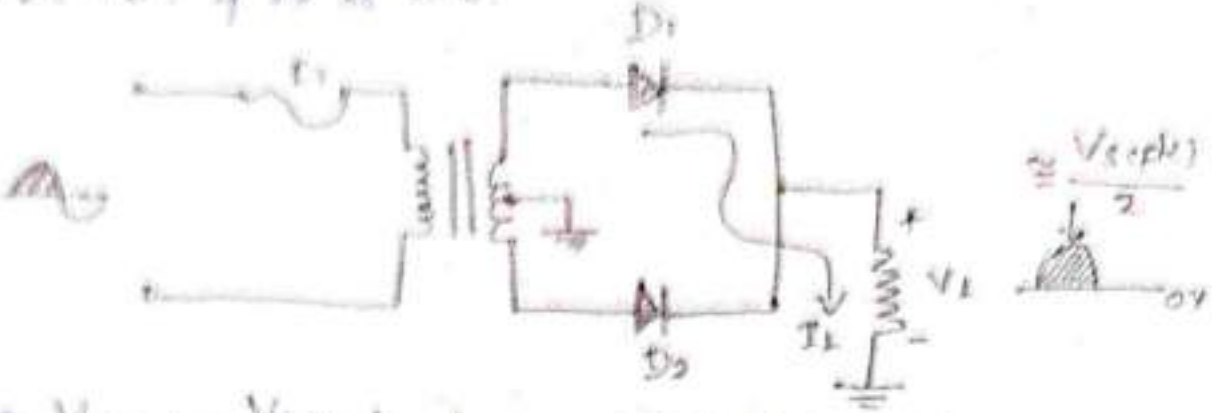
Full-wave Rectifier:

→ The full-wave rectifier consists of two diodes that are connected as shown in fig below.
→ The transformer shown is a center-tapped transformer. It has a lead connected to the center of the secondary winding.
→ The voltage from the center tap to each of the outer winding terminals is equal to half the secondary voltage.

Circuit Operation for positive FWR:

→ during the positive half-cycle of the input,

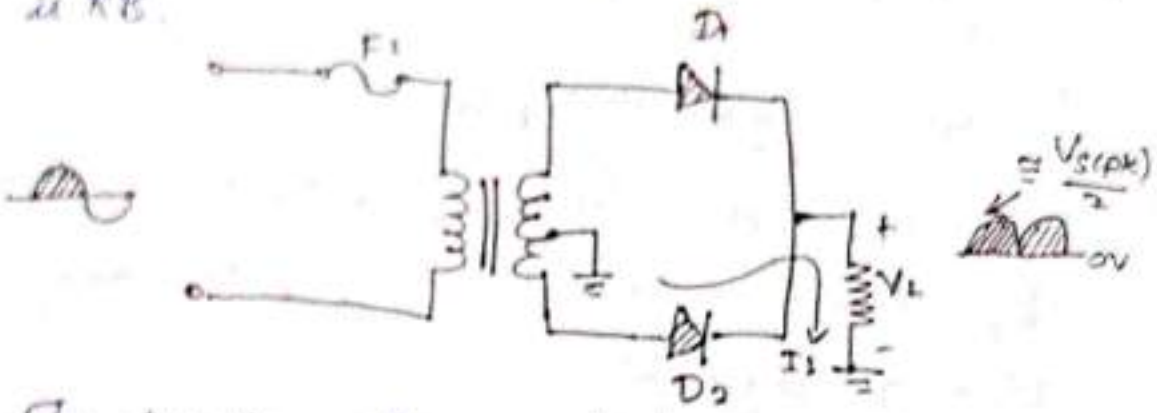
D_1 is FB & D_2 is RB.



→ $V_{L(pk)} = \frac{V_{s(pk)}}{2}$ for an ideal diode.

→ $V_{L(pk)}$ is half of $V_{s(pk)}$ because it is center-tapped transformer.

→ when the input polarity inverse, D_2 is FB & D_1 is RB.



→ The direction of current has not changed, so another positive half-cycle is produced across the load.

Load Voltage & load current:

→ The peak voltage for a FWR using the practical diode model is

$$V_{L(pk)} = \frac{V_{s(pk)}}{2} - 0.7V$$

→ The FWR produces twice as many output pulses (per input cycle) as the HWR.

→ The average load voltage for the FWR is

$$V_{ave} = \frac{2V_{L(pk)}}{\pi} = 0.637 V_{L(pk)}$$

The peak load current,

$$I_{L(pk)} = \frac{V_{s(pk)}}{R_L}$$

Peak Inverse voltage (PIV):

The peak inverse voltage is,

$$PIV \cong 2V_{s(pk)} \cong V_{s(pk)}$$

The peak load voltage supplied by the FWR is approximately half the secondary voltage V_s

Transformer utilization factor (TUF):-

The average TUF in a FWR is determined by considering the primary & secondary winding separately.

$$TUF = 0.693$$

Form factor:

$$F.F = \frac{\text{rms value of the o/p voltage}}{\text{average value of the o/p voltage}}$$

$$F.F = \frac{V_m/\sqrt{2}}{2V_m/\pi} = 1.11$$

Peak factor:

$$\text{Peak factor} = \frac{\text{Peak value of the o/p voltage}}{\text{rms value of the o/p voltage}}$$

$$P.F = \frac{V_m}{V_m/\sqrt{2}} = \sqrt{2}$$

Ripple factor:

$$\Gamma = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1} = \sqrt{\left(\frac{V_m/\sqrt{2}}{2V_m/\pi}\right)^2 - 1}$$

$$\boxed{\Gamma = 0.482}$$

Efficiency (η):

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{(V_{dc})^2/R_L}{(V_{rms})^2/R_L} = \frac{(2V_m/\pi)^2}{(V_m/\sqrt{2})^2}$$

$$\boxed{\eta = \frac{P_{dc}}{P_{ac}} = 81.2\%}$$

The maximum efficiency of a FWR is 81.2%.

Full-Wave Bridge Rectifier:

The bridge rectifier is most commonly used full-wave rectified for several reasons.

i) It does not require the use of a center-tapped transformer.

ii) The peak output voltage is twice to that of conventional FWR, So higher d.c output voltage.

Basic circuit Operation:

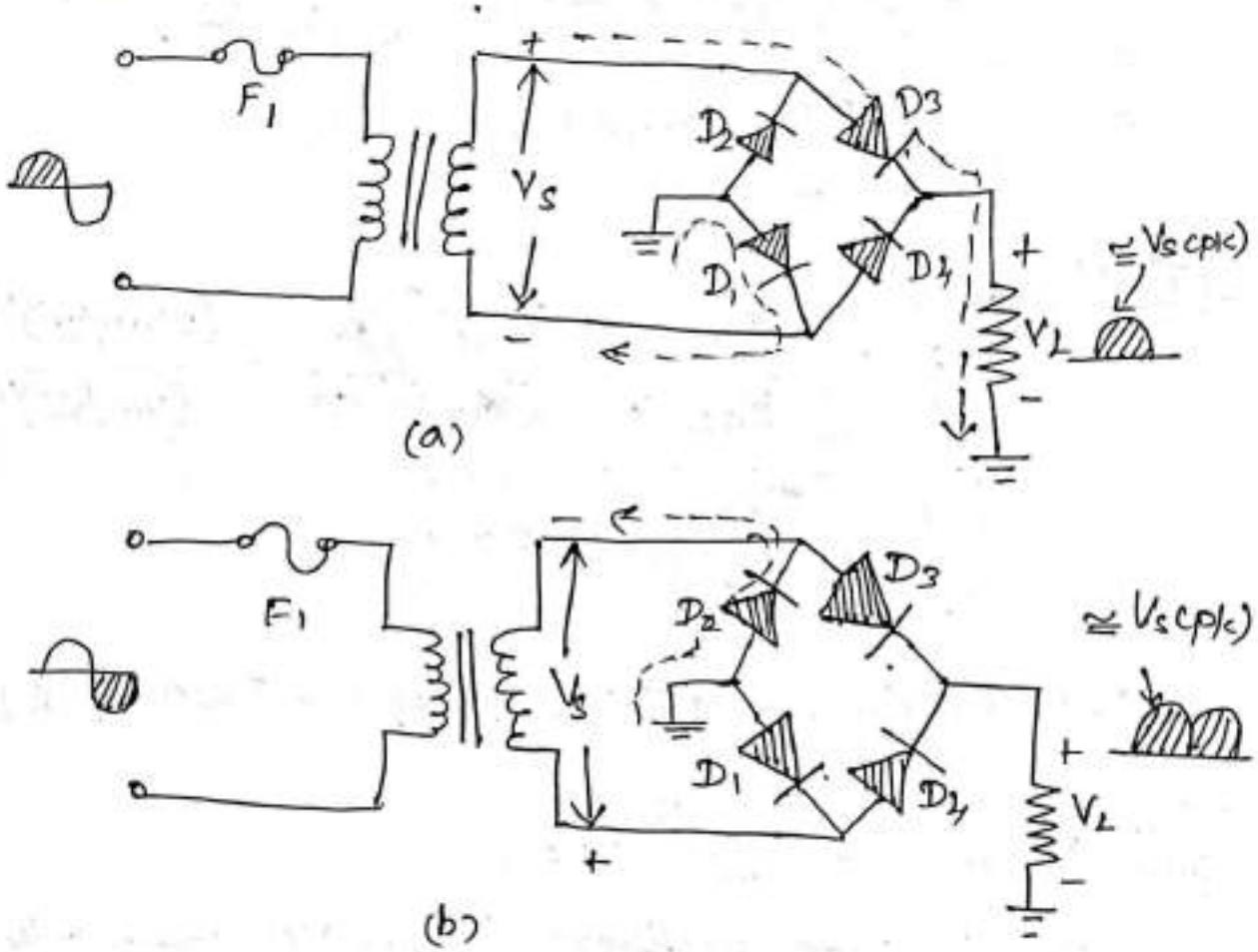
→ The bridge rectified consists of four diodes

→ The bridge rectifier alternates conduction between two diode pairs.

→ During the positive half-cycle of the input, D_1 & D_3 will conduct & during negative half-cycle D_2 & D_4 will conduct.

→ The current direction through the load & the

Polarity of the load voltage has not changed in both cases.



Load voltage & Load current:

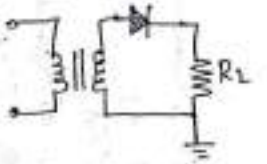
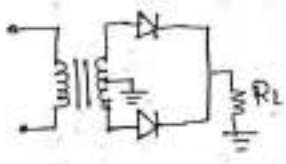
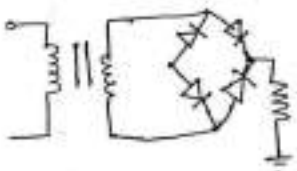
→ The bridge rectified does not require the use of a center-tapped transformer. Assuming the diodes are ideal, the peak output voltage is

$$V_{L(pk)} \cong V_{s(pk)} \quad \text{(ideal)}$$

→ In practical cases, there are two conducting diodes in series with the load, so the peak load voltage is,

$$V_{L(pk)} = V_{s(pk)} - 1.4V \quad \text{(practical)}$$

COMPARISON OF RECTIFIERS

Rectifier Type	Half-wave rectifier	full-wave Rectifier	Bridge Rectifier
Schematic diagram			
Typical output waveform			
no. of diodes	1	2	4
Peak o/p voltage	$V_{s(PK)} - 0.7V$	$V_{s(PK)} - 0.7V$	$V_{s(PK)} - 1.4V$
DC o/p voltage (no load)	$V_{L(PK)} / \pi$	$2V_{L(PK)} / \pi$	$2V_{L(PK)} / \pi$
PIV	$V_{s(PK)}$	$2V_{s(PK)}$	$V_{s(PK)}$
Form factor	1.57	1.11	1.11
Peak factor	2	$\sqrt{2}$	$\sqrt{2}$
TUF	0.287	0.693	0.812
Ripple factor	1.21	0.48	0.48
Maximum efficiency	40.6%	81.2%	81.2%

A HWR is supplied from 230V, 50Hz supply with stepdown ratio of 3:1 to a resistance load of 10KΩ. Diode forward resistance is 75Ω, which transformer, secondary resistance is 10Ω. Calculate maximum, average, RMS values of current, DC output voltage, η, & Ripple factor

Solution:

$$E_{p\,rms} = 230$$

$$\frac{N_2}{N_1} = \frac{E_{s(rms)}}{E_{p(rms)}} = \frac{1}{3} = \frac{E_{s(rms)}}{230}$$

$$E_{s(rms)} = 76.67V$$

$$E_m = \sqrt{2}\, E_{s(rms)} = 108.42V$$

$$I_m = \frac{E_m}{r_s + r_f + R_L} = 10.75mA$$

$$I_{av} = I_m/\pi$$

$$I_{av} = 3.422mA$$

$$I_{rms} = I_m/2$$

$$I_{rms} = 5.375\,mA.$$

$$(V_{dc})_{NL} = \frac{E_m}{\pi} = 1$$

% Regulation $= R_f/R_L \times 100\%$.

% Regulation $= 0.85\%$.

$$I_{dc} = \frac{I_m}{\pi}$$

$$E_{dc} = I_{dc} \times R_L$$

$$E_{dc} = 34.22V$$

$$\eta = (V_m/\pi)^2/(V_m/2)^2$$

$$\eta = 40.19\%.$$

Ripple factor $= \sqrt{(\pi/2)^2 - 1} = 1.21$

A FWR is fed from centre tap transformer. Secondary winding RMS voltage from either end of secondary to centre tap is 30V. Diode for $r = 2\Omega$, half secondary is 8Ω. for a load of $1k\Omega$ calculate.

a) Power delivered to load
b) % regulation at full load
c) efficiency.

Solution:

$E_s = 30V$, $R_f = 2\Omega$, $R_s = 8\Omega$, $R_L = 1k\Omega$

$E_m = E_s\sqrt{2} = 30\sqrt{2} = 40.426V$

$I_m = E_m / R_f + R_L + R_s = 42mA$

$I_{dc} = 2I_m/\pi = 26.74mA$

Power delivered to load $= I_{dc}^2 R_L = 0.715W$

V_{dc}, no load $= \frac{2E_m}{\pi} = 27V$

V_{dc}, load $= I_{DC} R_L = 26.74V$

% Regulation $= R_f / R_L \times 100$

% Regulation $= 0.97\%$

Efficiency $= 80.2\%$.

ZENER DIODE - VI Characteristics:

Zener diode:

A diode that is designed to work in the reverse breakdown region of its operating curve.

Reverse breakdown voltage:

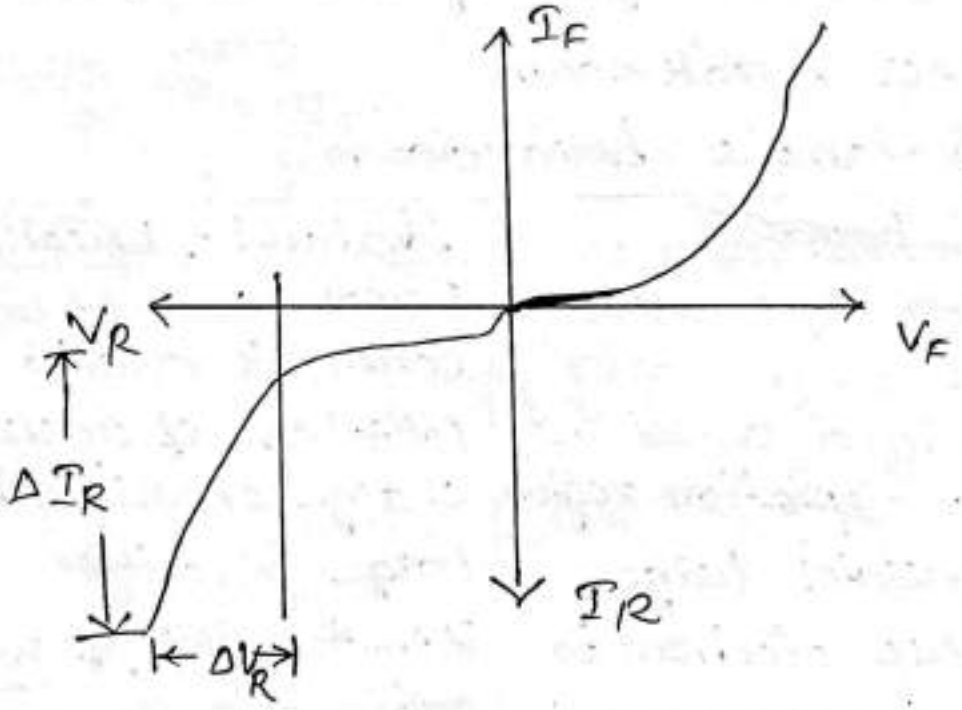
The reverse minimum V_R that causes a device to breakdown & conduct in the reverse direction.

→ when V_{BR} is reached, two things happen

i) The diode current increases drastically.

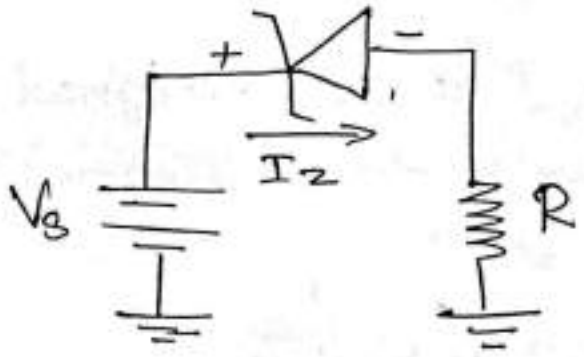
ii) The reverse voltage across the diode (V_R) remains relatively constant.

Zener characteristic curve:



→ The forward operating curve is same as PN diode.

→ The zener current is normally in the direction as shown in fig.



→ when a zener is operating in reverse operating region, the device is nearly constant & equal to V_Z rating (1.8V to several hundred volts)

Zener voltage (V_Z):

The approximate voltage across a zener when operated in reverse break down.

Diode Breakdown:

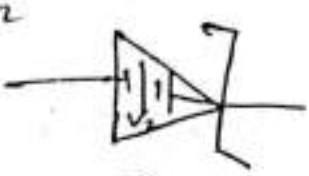
There are two types of reverse breakdown

i) zener breakdown

ii) Avalanche breakdown.

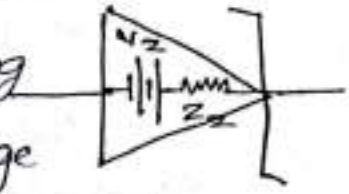
Sino	Zener Breakdown	Avalanche breakdown
1.	Breaking of covalent bonds is due to intense electric field across the narrow depletion region. This generates large no. of free electrons to cause breakdown.	Breakdown of covalent bonds is due to collision of accelerated charge carriers having large velocities & Kinetic energy with adjacent atoms. The process is called carrier multiplication.

Ideal: This model considers the zener to be a voltage source $= V_Z$. when placed in circuit it opposes applied circuit voltage.



Ideal

Practical: This model includes a series resistor Z_Z & is used for predicting the response of the diode to a change in circuit current.



Practical

Applications: The voltage across a zener diode operated in reverse region is relatively constant over a range of component current values despite variations in load current or input voltage, so it is useful as voltage regulator.

→ fixing reference voltages in electronic circuits such as power supplies & transistor biasing.
→ clippers in waveshaping circuits.
→ Square wave generators.

Zener diode as Voltage Regulator:

A voltage regulator is a circuit that maintains the output of a DC power supply constant against variation in

→ Input AC voltage
→ load current

The circuit diagram of zener regulator is illustrated below.

The operation of zener regulator can be explained by seperately considering the variations in input supply & the load current.

These two cases are explained next.

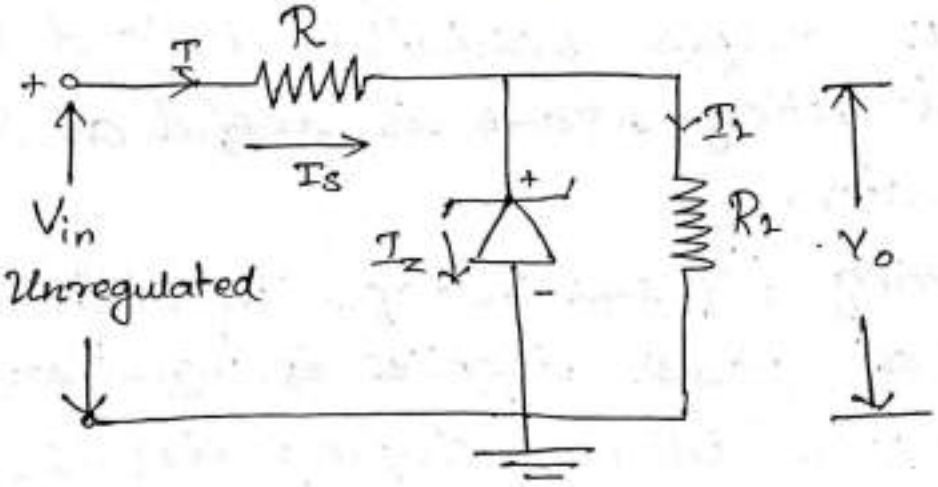


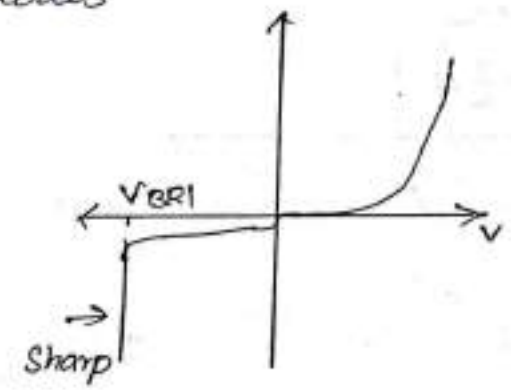
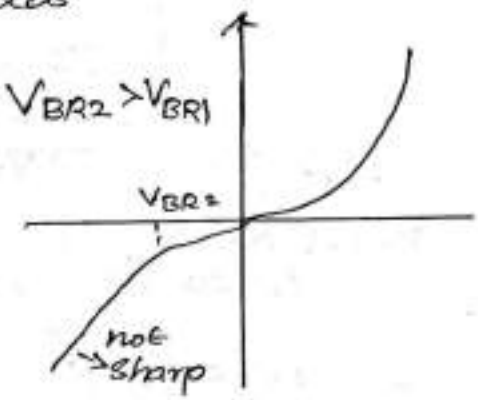
fig: zener regulator with varying voltage regulator

i) If R_L increases I_L decreases, to keep constant I_2 increases,

$$R_L \uparrow \longrightarrow I_{L(min)} \downarrow \longrightarrow I_{2(max)} \uparrow \quad -①$$

$$I_{L(min)} = I - I_{2(max)}$$

ii) If R_L decreases. I_L increase, to keep constant I_2 decreases,

2	This occur for zener diodes with V_{BR} less than 6V.	This occur for zener diodes with V_{BR} greater than 6V.
3.	The temperature co-efficient is negative	The temperature co-efficient is positive.
4.	The breakdown voltage decreases as junction temperature increases	The breakdown voltage increases as junction temperature increases
5	The V-I characteristics is very sharp in break--down region.	The V-I characteristics is not as sharp as in Zener breakdown in the breakdown region.
6	Occurs for heavily doped diodes	Occures for lightly doped diodes
7.		
8.	Low V_z ratings	High V_z ratings

Zener operating characteristics:

Zener knee current (I_{ZK}):

The minimum value of zener current required to maintain voltage regulation.

Maximum zener current (I_{ZM})

The maximum allowable value of zener reverse current.

Zener test current (I_{ZT})

The value of zener current at which the nominal values of the component are measured

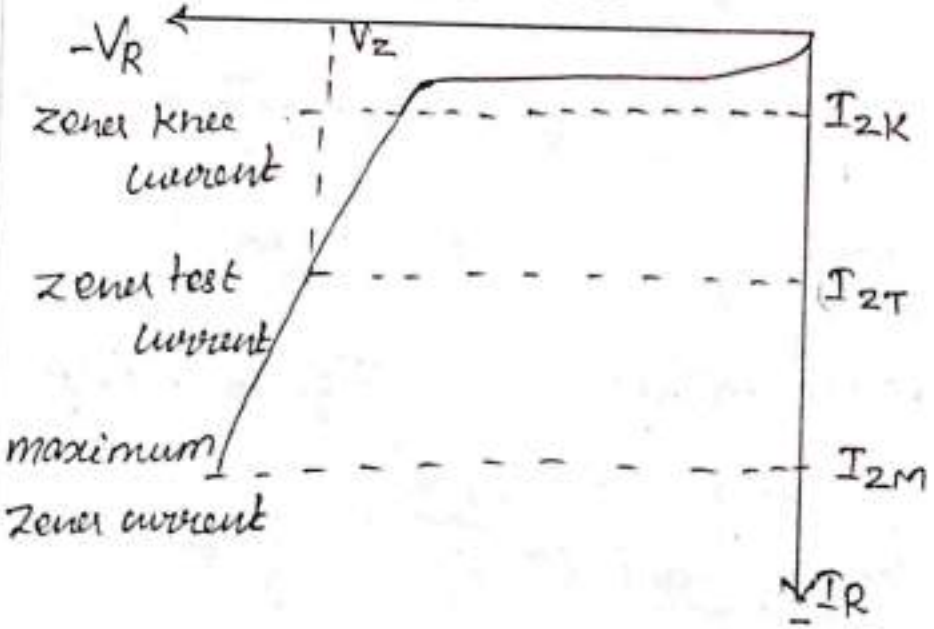
Static reverse current (I_R)

The reverse current through a diode when V_R is less than the components reverse breakdown voltage.

Zener impedance (Z_z):

The zener diodes opposition to change in current.

$$Z_z = \frac{\Delta V_z}{\Delta I_z}$$



Zener equivalent circuits:

→ There are basically two equivalent circuits for the zener diode.

$R_L \downarrow \longrightarrow I_{L(max)} \uparrow \longrightarrow I_{Z(min)} \downarrow$

$$I_{L(max)} = I - I_{Z(min)} \quad \text{——(2)}$$

iii) The maximum power dissipation in zener remain same as,

$$P_D = V_Z I_{Z(max)} \quad \text{——(3)}$$

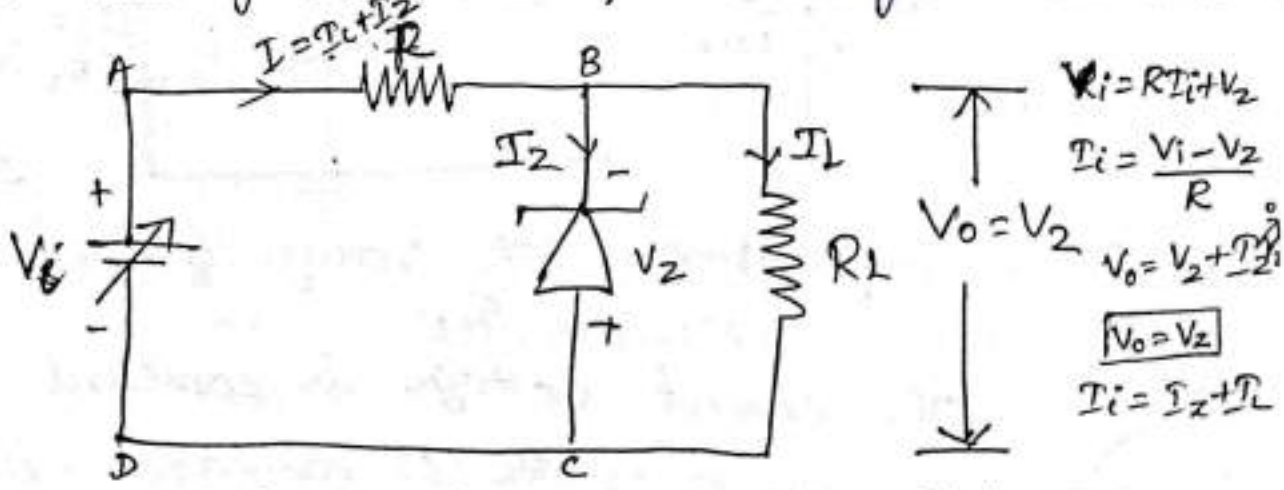
Regulation With Varying input Voltage:

The input Voltage V_i is shown as a Vauiable Voltage (Dc Supply).

This input voltage is unregulated, as it vauies due to the vauiations in the input. AC Supply to the rectifier.

$V_i > V_Z$, The zener diode operates in reverse - biased region

The necessary condition for the operation of this circuit is that the zener diode should always remain in the breakdown region. Through out the operation of the circuit



Zener regulator with vaugin input Voltage.

It can be seen that the output is,

$V_o = V_z$ is constant.

$$I_L = \frac{V_o}{R_L} = \frac{V_z}{R_L} = \text{constant}$$

$$I = I_L + I_z \quad \text{—— ①}$$

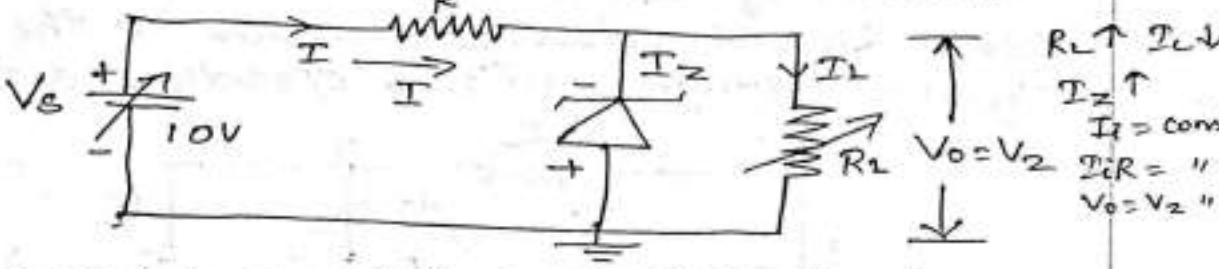
Now if V_o increases, then the total current I increases, But I_L is constant as V_z is constant. Hence the current I_z increases to keep I_L constant

If V_o decreases, then current I decreases. But to keep I_L constant, I_z decreases.

Regulation varying with load:

The circuit conditions for the zener regulator with varying load current is illustrated.

The load current increases when the load resistance decreases, and the load current decreases if the load resistance increases..



Zener regulator with varying load resistor R_L.

The input voltage is constant while the load resistance R_L is variable. As V_s is constant & $V_o = V_z$ is constant, then for constant R the current I is constant. $I = \frac{V_{in} - V_z}{R}$

4.9.2 V-I Characteristics of Zener Diode

- In the forward biased condition, the normal diode and the zener diode operate in similar fashion.
- But zener diode is designed to operate in reverse breakdown region hence its reverse V-I characteristics is important.
- When the reverse voltage is applied to zener diode, initially current is small, which is it's reverse saturation current.
- At a certain reverse voltage, the reverse breakdown occurs and current in the zener diode increases rapidly. The sharp change in the zener current is called **knee** or **zener knee** of the reverse characteristics.
- The reverse bias voltage at which the breakdown occurs is called **zener breakdown voltage**, denoted as V_Z. This value is carefully designed by controlling the doping level during manufacturing.
- The V-I characteristics of zener diode is shown in the Fig. 4.9.2.

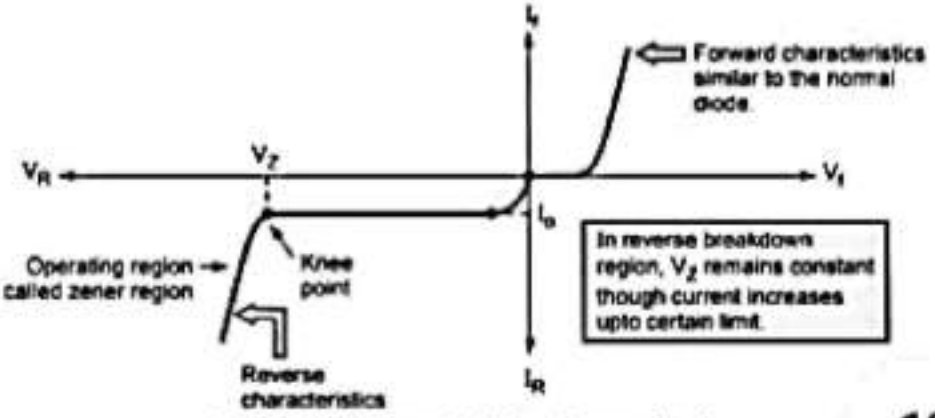
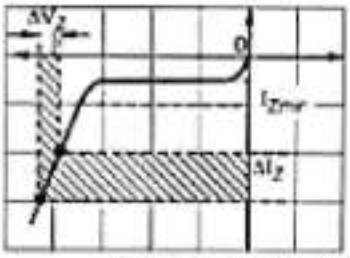


Fig. 4.9.2 V-I characteristics of zener diode

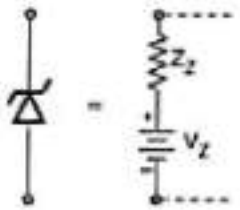
- For zener diodes, practically two currents are specified. The I_{Zmin} is minimum zener diode to maintain its reverse breakdown operation.
- The I_{Zmax} is the maximum current which zener diode can take safely maintaining its reverse breakdown operation, i.e. constant V_Z across it. If reverse current exceeds this value, the diode may get damaged due to excessive power dissipation.

4.9.3 Equivalent Circuit of a Zener Diode

- Practically though very small, zener has its internal resistance.
- In the zener region, this resistance is called **dynamic resistance** of the zener denoted as Z_z.
- Practically zener region is not exactly vertical. The small change in zener current ΔI_Z produces a small change in zener voltage ΔV_Z. The ratio of ΔV_Z to ΔI_Z is called zener resistance Z_Z. This is shown in the Fig. 4.9.3 (a).
- Hence practically zener equivalent circuit is shown with a battery of V_Z alongwith a series resistance Z_Z as indicated in the Fig. 4.9.3 (b).



(a) Dynamic resistance



(b) A.C. equivalent circuit

Fig. 4.9.3

- Mathematically zener resistance is given by,

$$Z_Z = \frac{\Delta V_Z}{\Delta I_Z} = \frac{1}{\left[\frac{\Delta I_Z}{\Delta V_Z}\right]} = \frac{1}{\left[\begin{array}{l}\text{Slope of the reverse}\\ \text{characteristics in}\\ \text{zener region}\end{array}\right]}$$

4.9.6 Applications of Zener Diode

- The various applications of zener diode are,

1. As a voltage regulator.
2. In voltage clipper circuits.
3. For controlling the output amplitude.
4. As a reference voltage in comparator circuits.
5. As a standard voltage source in calibrating the instruments.

BJT, JFET, MOSFET - Structure, operation, characteristics & Biasing UJT, Thyristor & IGBT - Structure & characteristics.

BJT:

The transistor is a multifunction Semiconductor device that, in conjunction with other circuit elements is capable of current gain, voltage gain & Signal power gain.

The transistor is therefore referred as an active device where as the diode is passive.

The basic transistor action is the control of current at one terminal by voltage applied across two other terminal of the device.

Types: The three basic transistor types includes,

i) Bipolar junction transistor (BJT)
ii) Metal oxide Semiconductor field effect transistor (MOSFET)
iii) Junction field effect transistor (JFET)

Geometry of BJT:

The bipolar transistors has three seperately doped regions & two PN junctions.

The three terminal connections are called the emitter, Base & collector. The Basic Structure & Symbol is Shown below.

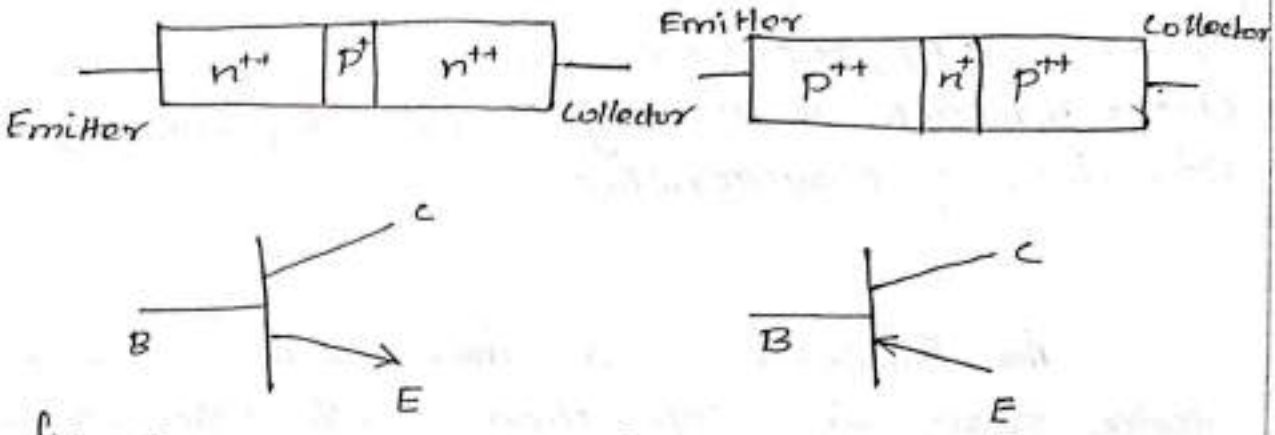


fig: ⓐ Block diagram ⓑ Circuit diagram

The width of the base region is small compared to the minority carrier diffusion length.

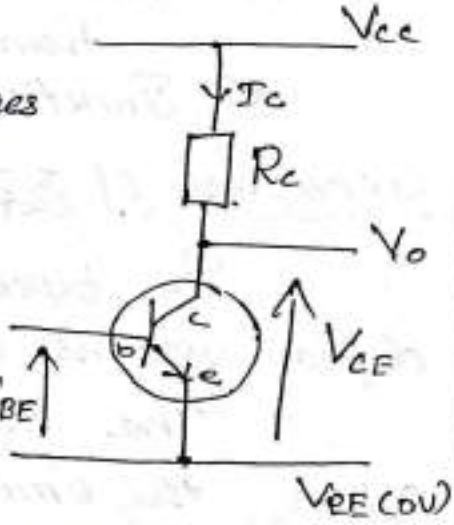
Bipolar transistor is not a symmetrical device.

Notation:

Bipolar transistors are 3 terminal devices
→ collector (C)
→ Base (b)
→ Emitter (E)

The base is the control input.

Diagram illustrate the notation used for labelling voltages & currents.



Relationship between the collector current & the base current in a bipolar transistor characteristic is approximately linear.

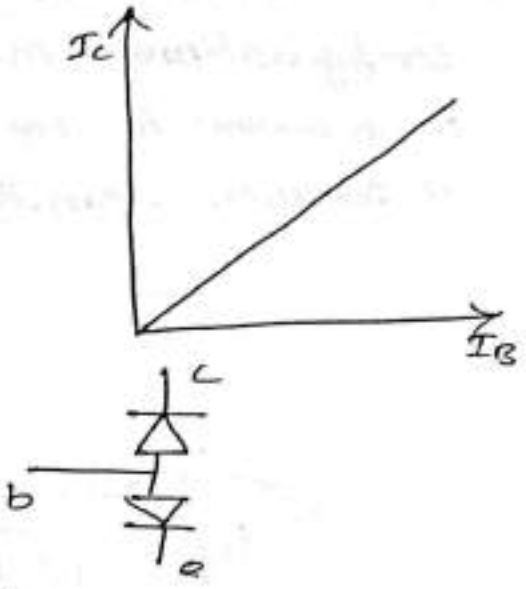
Magnitude of collector current is generally many time of the base current

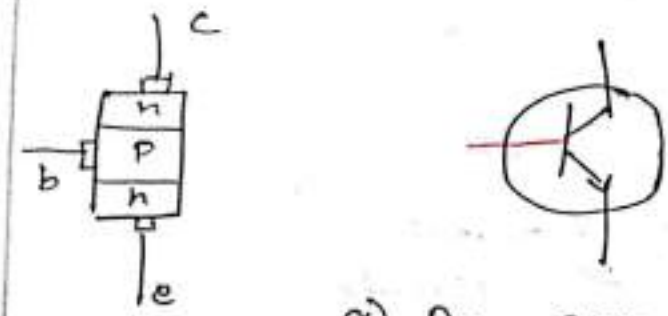
The device provides current gain.

construction:

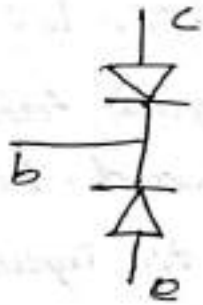
Two polarities,

npn & pnp

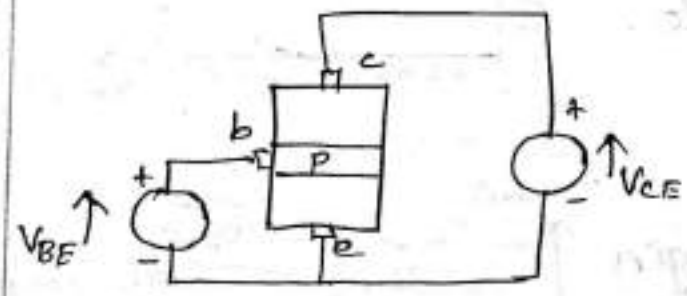


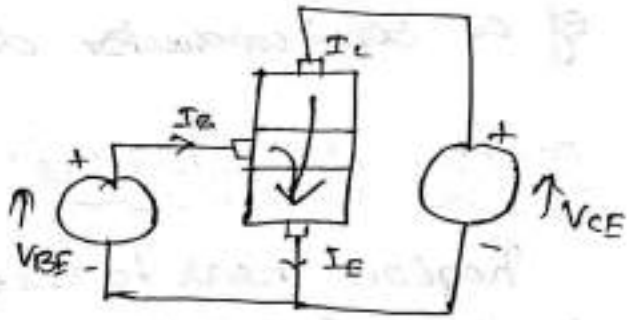


a) An npn transistor

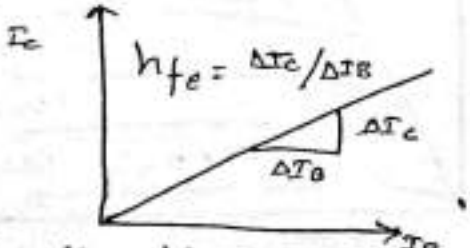


b) An pnp transistor

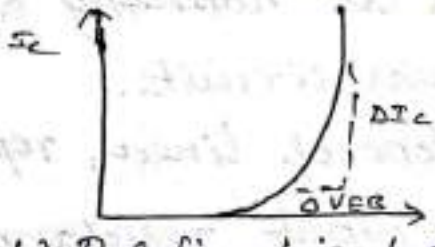




Behaviour can be described by the current gain h_{fe}, or by the transconductance, g_m of the device.



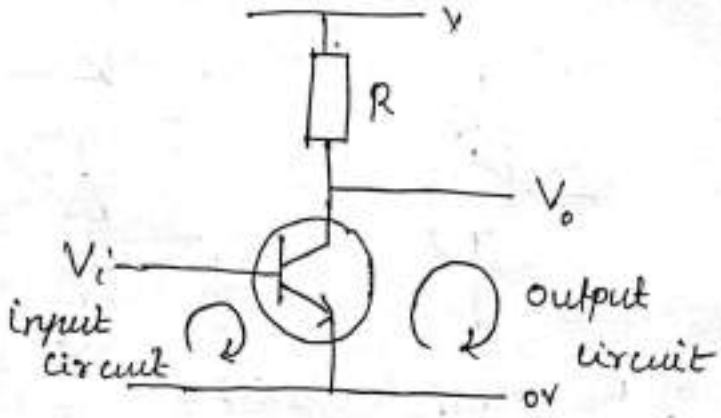
a) Relationship between output current & input current



b) Relationship between output current & input voltage.

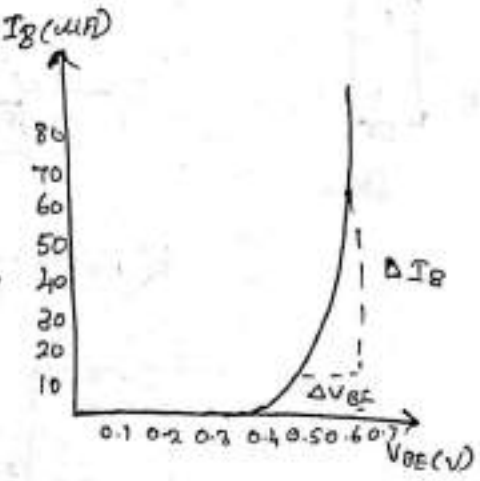
Transistor Configurations:

Transistors can be used in a numba of configurations most common is emitter termind is common to input & output circuits. This is a common-emitter configuration.



Input Characteristics

→ The input takes the form of a forward-biased pn Junction the input characteristic are therefore similar to those of a semiconductor diode.

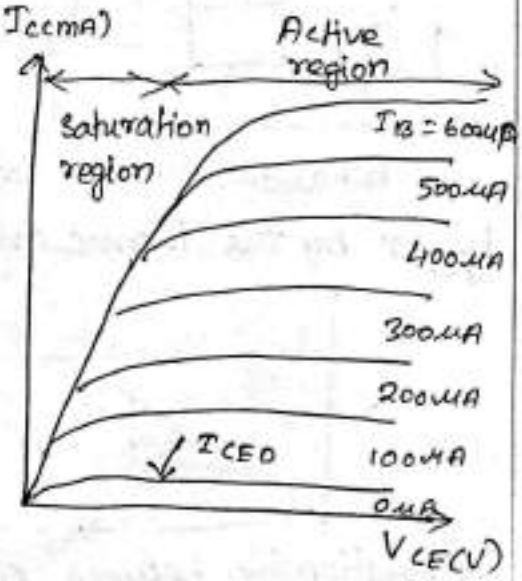


Output characteristics:

Region near to the origin is the Saturation region

This is normally avoided in linear circuits.

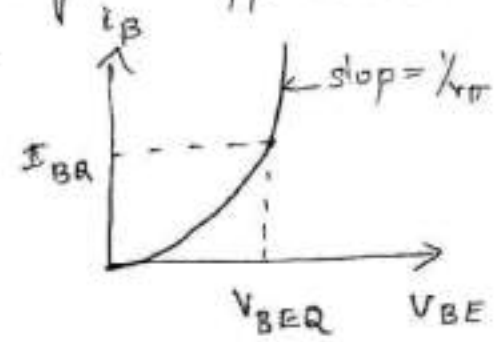
Slope of linear represents the output resistance.



Unit - II BJT Amplifiers

Small signal hybrid π equivalent

BJT as two port n/w, small signal i/p base current related to i/p voltage by



$$V_{be} = i_b r_\pi$$

$1/r_\pi$ = slope of $i_B - V_{BE}$ curve

i_b - time varying base current is given by

$$i_b = \left(\frac{I_{BQ}}{V_T}\right)_{V_{be}} \times V_{be}$$

$$r_\pi = \frac{V_{be}}{i_b} = \frac{V_T}{I_{BQ}} = \frac{\beta V_T}{I_{CQ}}$$

. The resistance r_π is called diffusion resistance or base-emitter input resistance.

The output collector current is a function of base emitter voltage and independent of collector-emitter voltage. The relation is

$$\Delta i_c = \frac{\partial i_c}{\partial V_{BE}}\bigg|_{Q\,pt} \Delta V_{BE}$$

$$i_c = \frac{\partial i_c}{\partial V_{BE}}\bigg|_{Q pt} \cdot V_{be}$$

$$i_c = I_S \exp\left(\frac{V_{BE}}{V_T}\right)$$

$$\frac{\partial i_c}{\partial V_{BE}}\bigg|_{Q pt} = \frac{1}{V_T} \cdot I_S \exp\left(\frac{V_{BE}}{V_T}\right)\bigg|_{Q pt} = \frac{I_{CQ}}{V_T}$$

term $I_S \exp\left(\frac{V_{BE}}{V_T}\right)$ is I_{CQ} at Q pt.

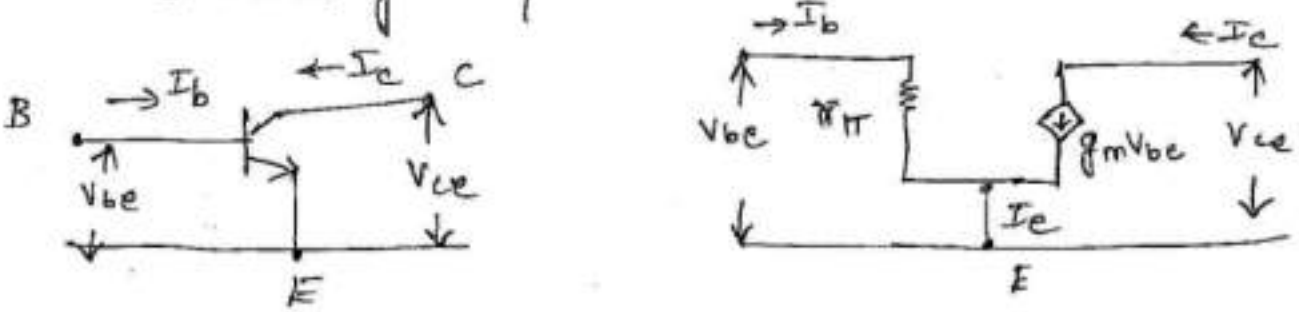
The term $\frac{I_{CQ}}{V_T}$ is conductance, relates collector current to voltage in base emitter ckt. the parameter is called transconductance given by

$$g_m = \frac{I_{CQ}}{V_T}$$

r_π, g_m → Q pt. parameters

r_π inv. prop. to I_{CQ}, $g_m \propto I_{CQ}$

Small signal parameters



Common-Emitter Current Gain

→ defined as β_{ac} (does not include leakage current)

β_{dc} → includes leakage current $\left(\frac{I_c}{I_B}\right)$

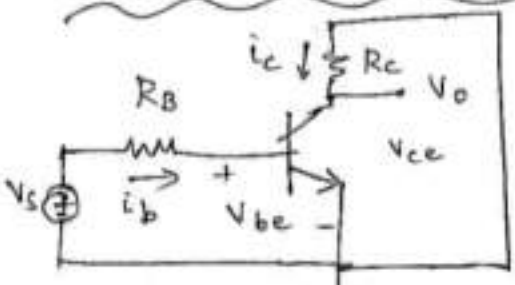
By neglecting leakage current

$$\beta_{dc} = \beta_{ac}$$

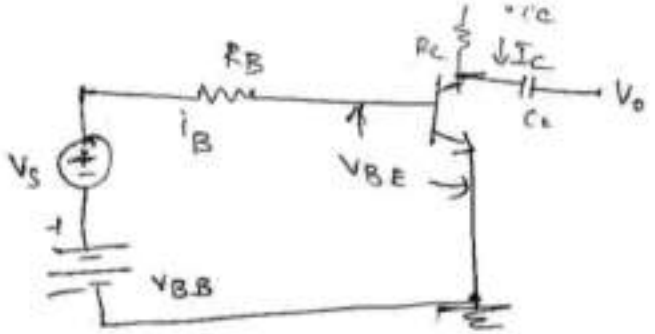
x/y r_π & g_m

$$r_\pi g_m = \left(\frac{\beta V_T}{I_{CQ}}\right)\left(\frac{I_{CQ}}{V_T}\right) = \beta$$

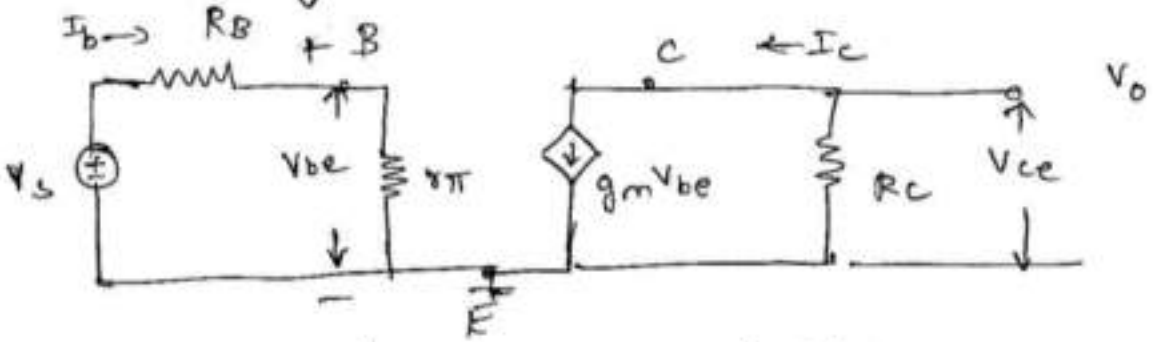
Common Emitter Amplifier



a.c equivalent



CE Amplifier



Small signal voltage gain (A_v)

defined as ratio of output signal voltage to input signal voltage. It is given by

$$A_v = \frac{V_o}{V_s}$$

$$V_o = V_{ce} = -(g_m V_{be}) R_c .$$

Applying voltage divider rule

$$V_{be} = \left(\frac{r_\pi}{r_\pi + R_B}\right) V_s$$

$$A_v = \frac{V_o}{V_s} = -(g_m R_c) \cdot \left(\frac{r_\pi}{r_\pi + R_B}\right)$$

Hybrid π equivalent ckt including Early Effect

According to Early Effect, I_c vary with V_{ce}.

$$r_o = \left.\frac{\partial V_{CE}}{\partial I_c}\right|_{@pt} = \frac{V_A}{I_{cQ}}$$

$$A_v = \frac{V_o}{V_s} = -g_m(r_o \| R_c)\left(\frac{R_1 \| R_2 \| r_\pi}{R_1 \| R_2 \| r_\pi + R_s}\right)$$

$$A_v = -g_m(r_o \| R_c)\left(\frac{R_i}{R_i + R_s}\right)$$

Output resistance (R_o)

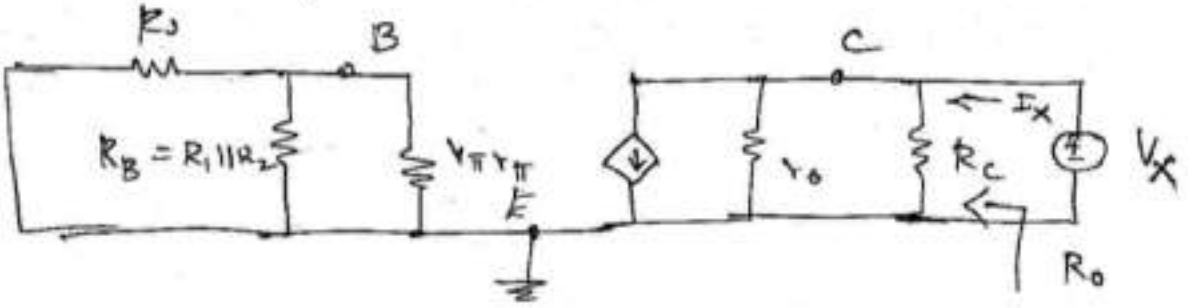
$V_s \rightarrow$ set to 0.

No excitation to i/p portion of circuit $V_\pi = 0$.

$g_m V_\pi = 0$ (o.c).

The o/p resistance looking back into o/p terminals is given by

$$R_o = \frac{V_x}{I_x} = r_o \| R_c$$



Early Effect

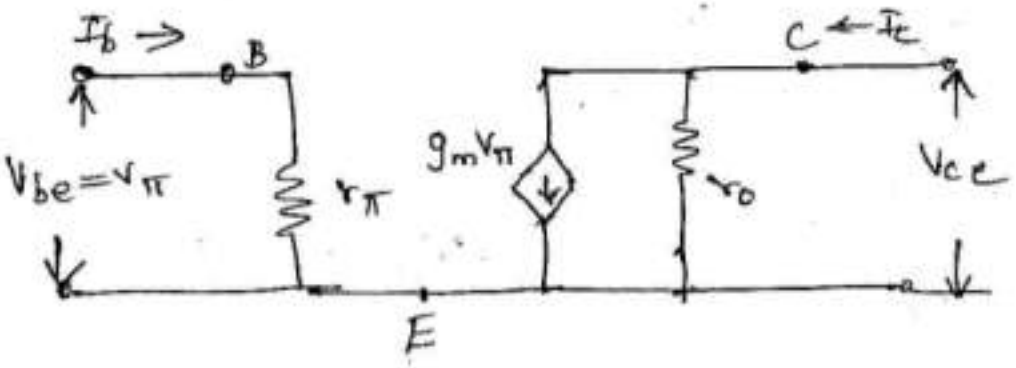
According to Early effect, the collector current does vary with collector emitter voltage. The relation between I_c and V_{CE} is given by.

$$r_o = \frac{\partial V_{CE}}{\partial i_c}\Big|_{Q\,pt} = \frac{V_A}{I_{CQ}}$$

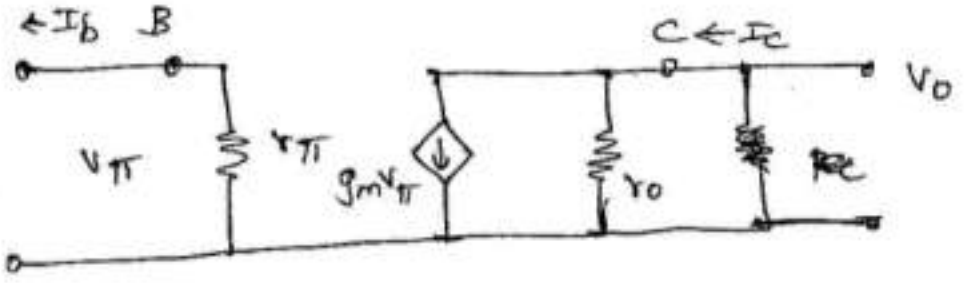
$V_A \rightarrow$ early voltage

This r_o is called small signal transistor o/p resistance

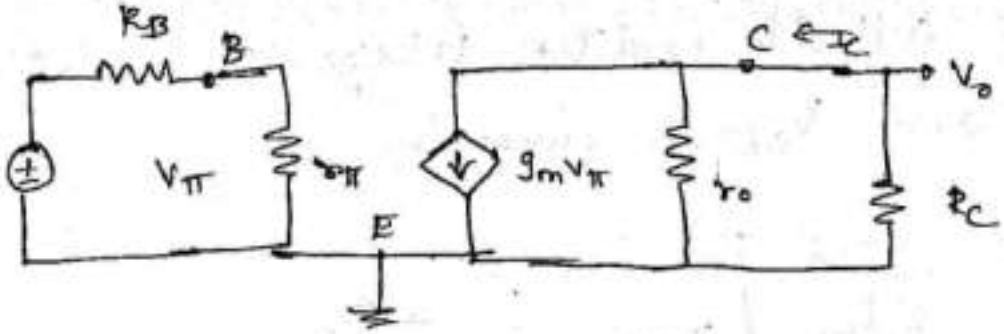
Hybrid π – equivalent (npn)



Hybrid π – equivalent pnp



CE amplifier with early effect



output voltage is

$$V_o = -g_m V_\pi (r_o \| R_C)$$

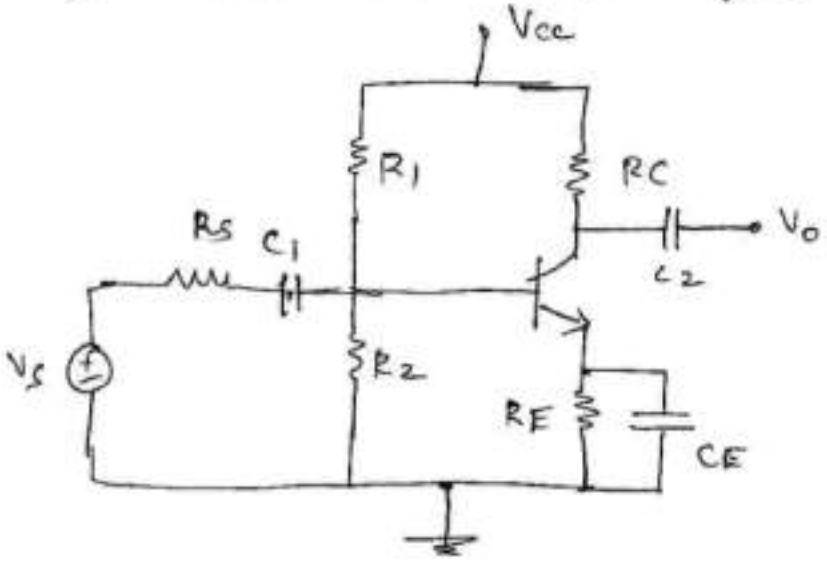
$$V_\pi = \left(\frac{r_\pi}{r_\pi + R_B}\right) V_s$$

$$A_v = \frac{V_o}{V_s}$$

$$= -g_m (r_o \| R_C)\left(\frac{r_\pi}{r_\pi + R_B}\right)$$

$$= \frac{-\beta}{r_\pi + R_B}(r_o \| R_C) \qquad \because g_m r_\pi = \beta$$

Small signal Analysis of common Emitter Amplifier

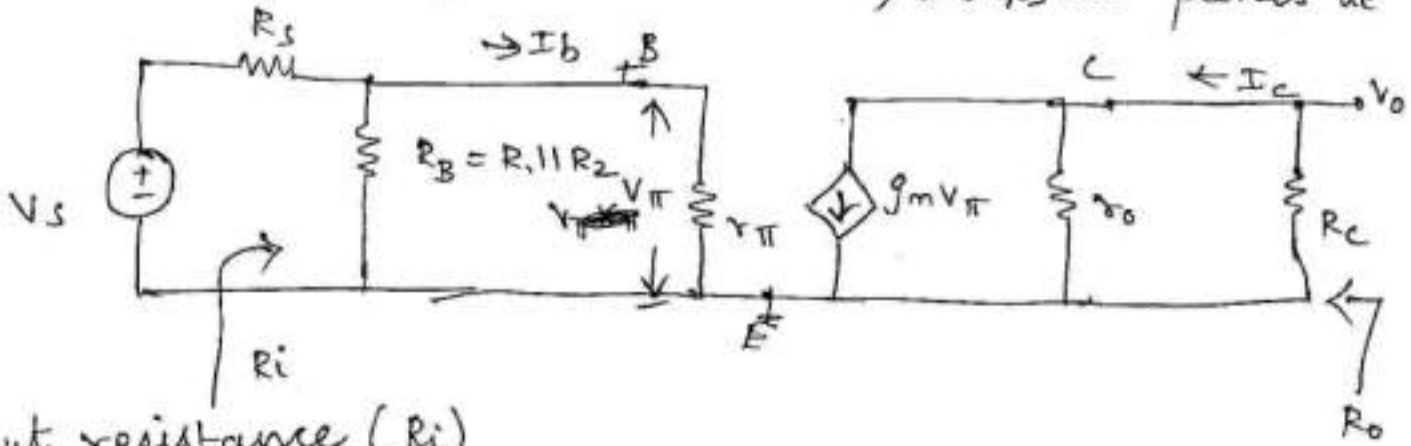


→ Signal source coupled into base by C_c (provides dc isolation

→ R_1, R_2, R_E - dc biasing

→ C_E → provides low reactance path if not inserted produces voltage drop across R_E ↓ V_o, ↓ gain

C_c → couples o/p of amp. to load, blocks dc passes ac



Input resistance (R_i)

$$R_i = R_1 \| R_2 \| r_\pi$$

Voltage gain (A_V)

$$V_o = -g_m V_\pi (r_o \| R_c) \quad \text{——} (1)$$

$$V_\pi = \left(\frac{R_1 \| R_2 \| r_\pi}{R_1 \| R_2 \| r_\pi + R_s} \right) V_s \quad -(2)$$

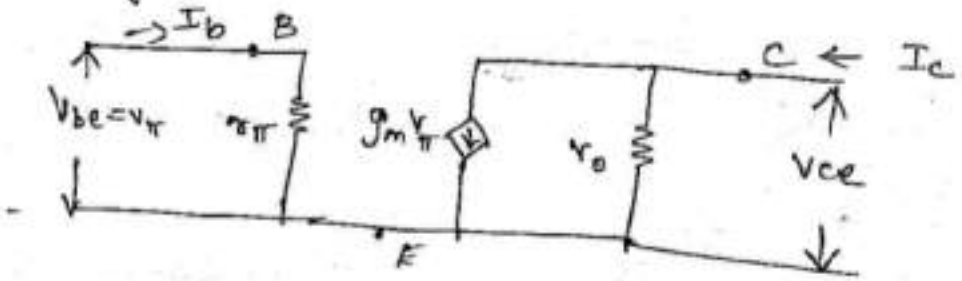
Sub (2) in (1)

$$V_o = -g_m (r_o \| R_c) \left(\frac{R_1 \| R_2 \| r_\pi}{R_1 \| R_2 \| r_\pi + R_s} \right) V_s$$

V_A = Early Voltage

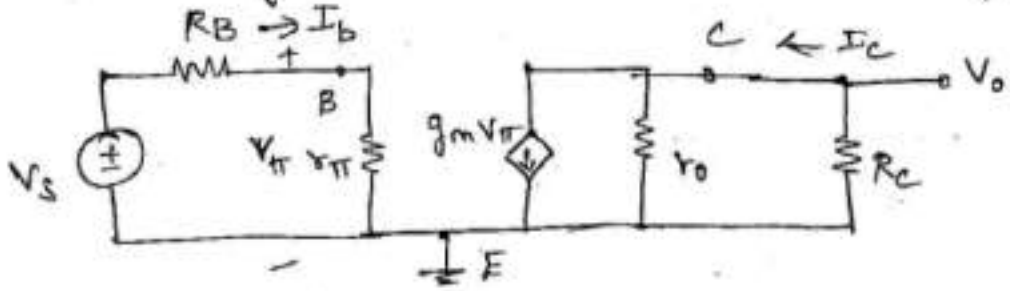
r_o is called small signal transistor o/p resistance.

considering r_o hybrid-π equivalent ckt is



for pnp transistor current direction are reversed

Small signal equivalent including early effect



the o/p voltage is given by

$$V_o = -g_m V_\pi (r_o \| R_c)$$

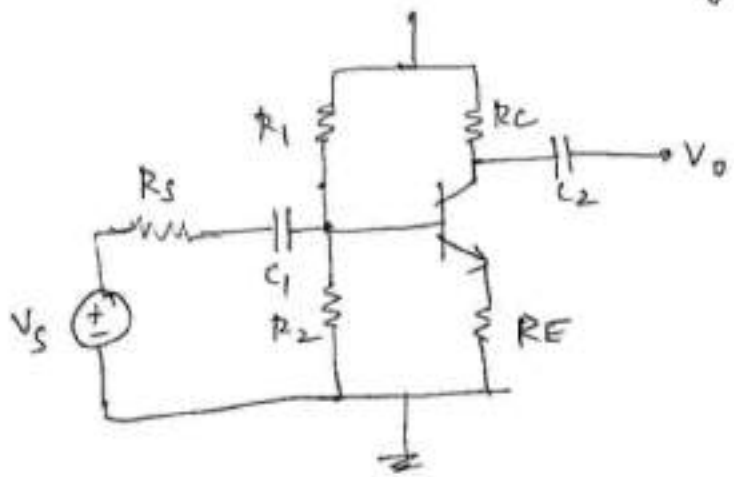
Applying voltage divider rule

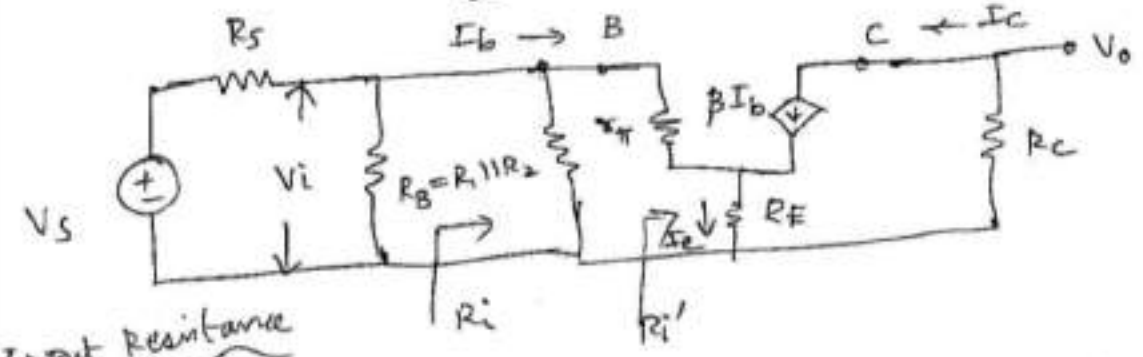
$$V_\pi = \left(\frac{r_\pi}{r_\pi + R_B}\right) V_S$$

$$A_V = \frac{V_o}{V_S} = -g_m (r_o \| R_c)\left(\frac{r_\pi}{r_\pi + R_B}\right)$$

$$= \left(\frac{-\beta}{r_\pi + R_B}\right)(r_o \| R_c) \qquad \because g_m r_\pi = \beta$$

Common Emitter with Unbypassed R_E





Input Resistance

$$V_i = I_b r_\pi + (1+\beta) I_b R_E$$

$$R_i' = \frac{V_i}{I_b} = r_\pi + (1+\beta) I_b R_E$$

$$R_i = R_1 \| R_2 \| R_i' = R_B \| R_i'$$

Voltage gain A_V

$$V_o = -(\beta I_b) R_C$$

$$A_V = \frac{V_o}{V_s} = \frac{V_o}{V_i'} \times \frac{V_i}{V_s}$$

$$V_i = I_b R_i' \quad \& \quad \frac{V_i}{V_s} = \frac{R_i}{R_i + R_s}$$

$$A_V = \frac{-\beta (I_b) R_C}{I_b R_i'} \times \frac{R_i}{R_i + R_s}$$

$$= \frac{-\beta R_C}{r_\pi + (1+\beta) R_E} \times \frac{R_i}{R_i + R_s}$$

if $R_i >> R_s$ & if $(1+\beta) R_E >> r_\pi$

$$A_V = \frac{-\beta R_C}{(1+\beta) R_E} \approx \frac{-R_C}{R_E}$$

Adv

1) A_V less independent on current gain (β)
2) R_E unbypassed $R_i >>$ $R_i >> R_s$ & reduces loading effect

Ac. Load line

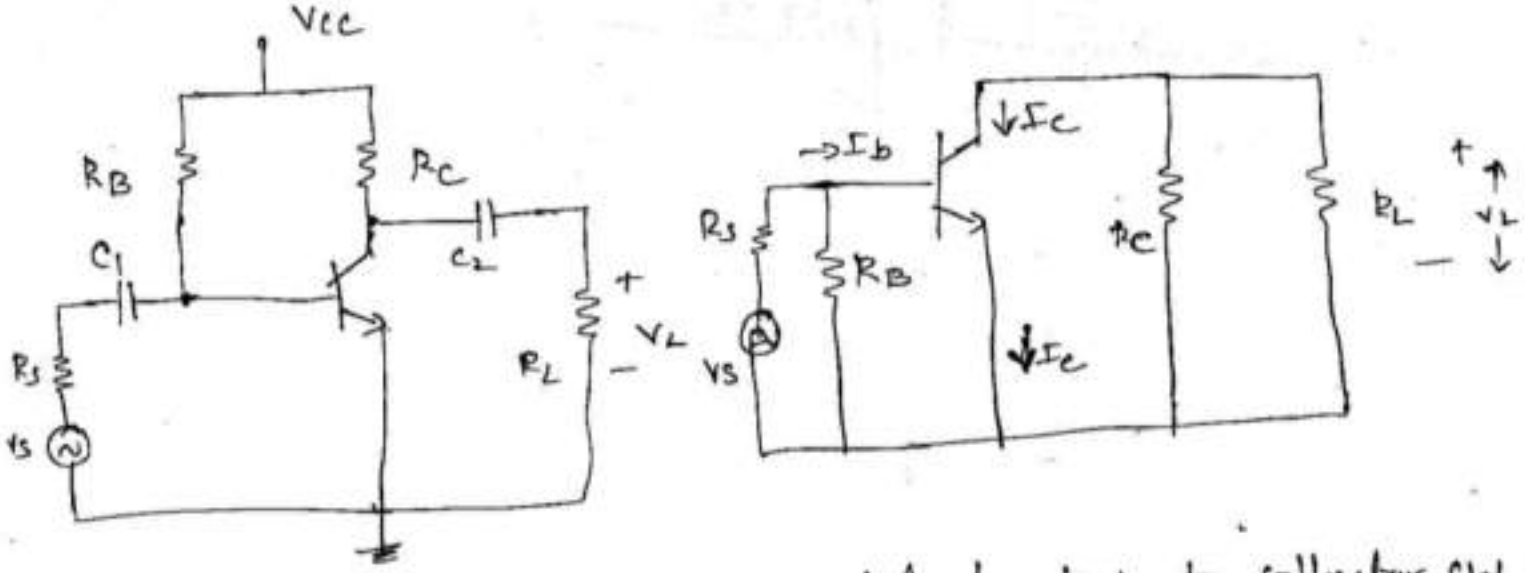
→ DC load line → relation b/w Q pt. & Tr. Characteristics

→ when capacitors are included in transistor, a new effective load line called ac load line exists. (gives relation b/w small signal response & Tr. characteristics)

For ac. analysis

* capacitors acts as short, dc source by short

The resultant ac. equivalent



The collector ckt resistance seen by dc bias current I_{CQ} is

$$R_{dc} = R_C$$

The collector ckt current sees collector ckt. resistance

$$R_{ac} = R_C \| R_L = \frac{R_C R_L}{R_C + R_L}$$

$$R_{ac} \neq R_{dc}$$

Apply KVL to collector ckt.

$$V_{ce} = I_c R_{ac} \quad — (1)$$

V_{ce} → ac. collector to emitter Volt

I_c : ac collector current

$$I_c = i_c - I_{CQ} \quad \& \quad V_{ce} = V_{CEQ} - V_c \quad — (2)$$

Sub (2) in (1)

$$V_{CEQ} - V_{CE} = (i_c - I_{CQ}) R_{ac}$$

i_c → Total instantaneous collector current

V_{CE} → Total instantaneous

Rearranging

$$i_c = \frac{V_{CEQ}}{R_{ac}} - \frac{V_{CE}}{R_{ac}} + I_{CQ} \quad -③$$

If $i_c = I_{CQ}$ is substituted in ② $V_{CE} = V_{CEQ}$.

This indicates ac load line intersect dc. load line at Q pt.

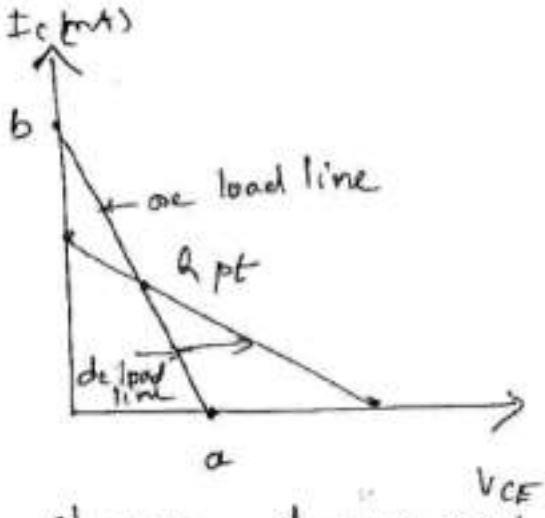
Point of intersection

Point a set $i_c = 0$ in ③

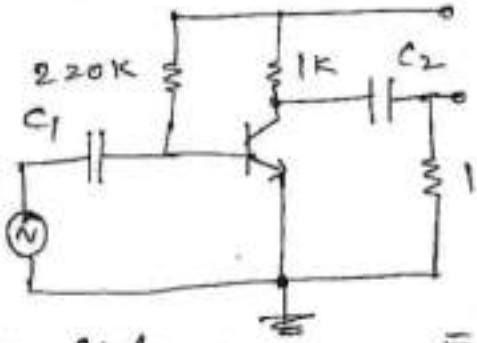
$$V_{CE\,max} = V_{CEQ} + I_{CQ} R_{ac}$$

Point b set $V_{CE} = 0$

$$I_{c\,max} = \frac{V_{CEQ}}{R_{ac}} + I_{CQ}$$



eg: 3.5.1 The ckt. of BJT amp. is shown draw ac & d.c load line. Also find Q pt. Assume $V_{BE} = 0.7$ & $\beta = 100$



$V_{cc} = 12V$

Step 1: obtain I_{CQ} & V_{CEQ} point A & point B

Apply KVL to base ckt.

$$V_{cc} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{cc} - V_{BE}}{R_B}$$

$$= \frac{12 - 0.7}{220K} = 51.36\,\mu A$$

$$I_{CQ} = \beta I_B = 100 \times 51.36\mu A = 5.136\,mA$$

Apply KVL to collecto ckt.

$$V_{cc} - I_c R_c - V_{CEQ} = 0$$

$$V_{CEQ} = V_{cc} - I_c R_c$$

$$= 12 - 5.136 \times 10^{-3} \times 1000 = 6.864\,V$$

Q pt. is $I_{CQ}, V_{CEQ} = 3.424\,mA, 6.864\,V$

Axes inter section

Point A: $V_{CE} = V_{cc} = 12V$ at $I_c = 0$

point B: $I_c = V_{cc}/R_{dc} = V_{cc}/R_c = \frac{12}{1K} = 12m.$

Step 2: obtain R_{ac}. Point a, b

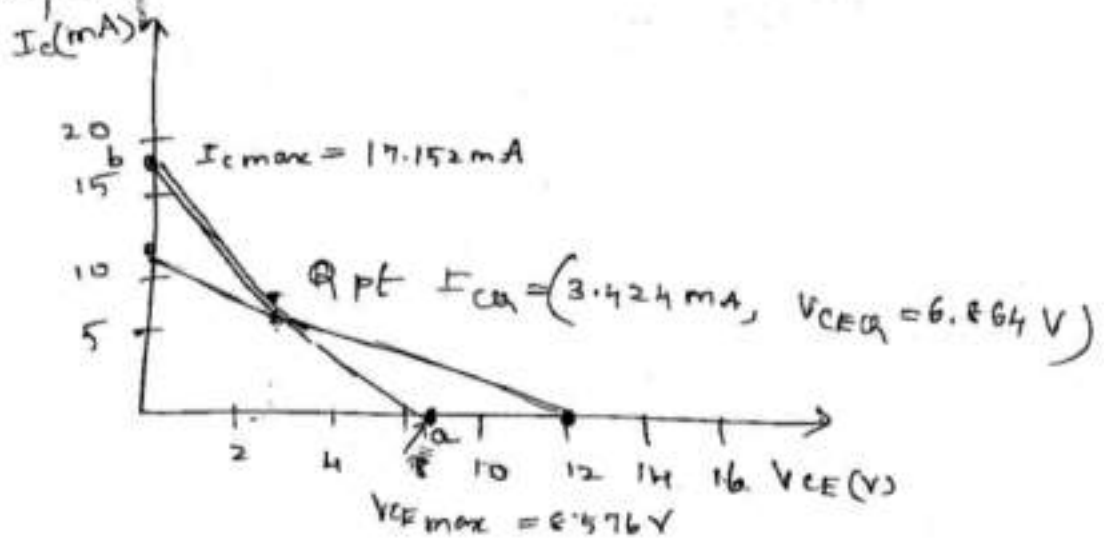
$$R_{ac} = R_c \| R_L = 1K \| 1K = 500\,\Omega$$

Point a: $V_{CE\,max} = V_{CEQ} + I_{CQ} R_{ac} = 6.864 + 3.424 \times 10^{-3} \times 500$

$= 8.576V$

Point b: $I_{cmax} = \frac{V_{CEQ}}{R_{ac}} + I_{CQ} = \frac{6.864}{500} + 3.424 \times 10^{-3} = 17.132mA$

Step 3:



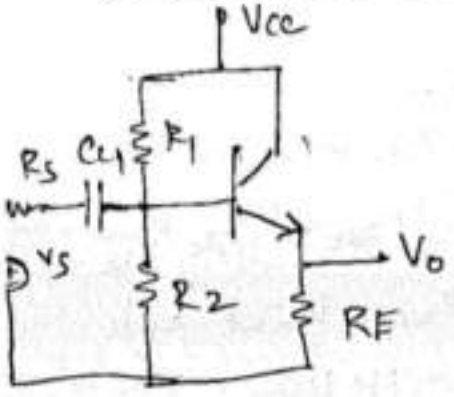
Voltage Swing Limitation

→ Symmetrical sinusoidal signals are applied to i/p get amplified sinusoidal signals at o/p

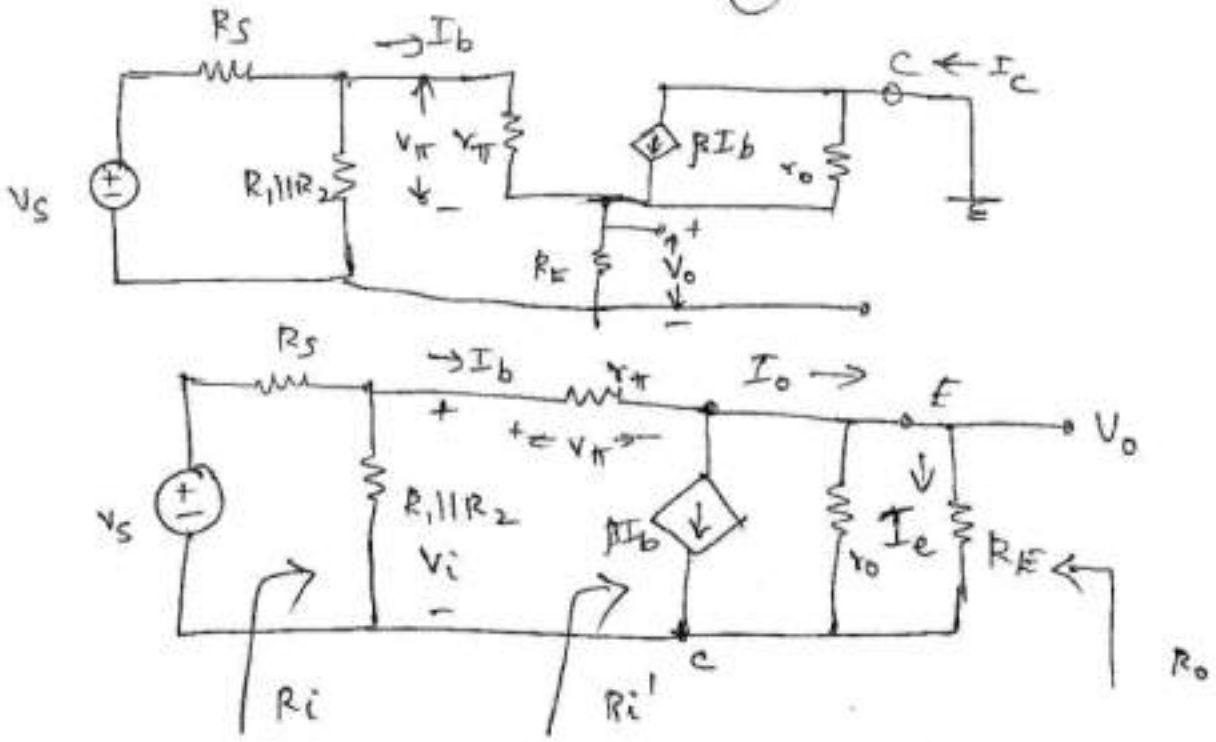
→ possible to obtain maximum o/p symmetrical ~~signal~~ swing amplifier can provide using ac load line

→ If o/p exceeds this limit, portion of o/p signal clipped resulting signal distortion

Common collector Amplifier Emitter follower.



(b)



Input Resistance (R_i)

$$I_o = I_b + \beta I_b = (1+\beta) I_b$$

$$V_o = I_o (r_o \| R_E) = (1+\beta) I_b (r_o \| R_E)$$

Apply KVL to base emitter loop

$$V_i = V_\pi + V_o = r_\pi I_b + (1+\beta) I_b (r_o \| R_E)$$

$$= I_b \left[r_\pi + (1+\beta)(r_o \| R_E) \right]$$

$$R_i' = \frac{V_i}{I_b} = r_\pi + (1+\beta)(r_o \| R_E)$$

$$R_i = R_1 \| R_2 \| R_i'$$

Voltage gain (A_v)

$$A_v = \frac{V_o}{V_s} = \frac{V_o}{V_i} \times \frac{V_i}{V_s} \qquad V_i = \left(\frac{R_i}{R_i + R_s} \right) V_s$$

$$= \frac{I_b (1+\beta)(r_o \| R_E)}{I_b \left[r_\pi + (1+\beta)(r_o \| R_E) \right]} \cdot \frac{R_i}{R_i + R_s}$$

$$A_V = \frac{(1+\beta)(r_o \| R_E)}{r_\pi + (1+\beta)(r_o \| R_E)} \cdot \frac{R_i}{R_i + R_s}$$

Current gain (A_i)

$$A_i = \frac{I_e}{I_i} = \frac{I_e}{I_o} \times \frac{I_o}{I_b} \times \frac{I_b}{I_i}$$

$$\frac{I_e}{I_o} = \frac{r_o}{r_o + R_E} \quad \text{— (1)}$$

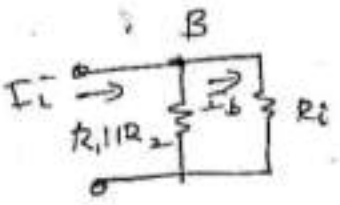
Apply KCL at middle node

$$I_o = (1+\beta)\, I_b$$

$$\frac{I_o}{I_b} = (1+\beta) \quad \text{— (2)}$$

Using collector divide at node B

$$I_b = \frac{R_1 \| R_2}{(R_1 \| R_2) + R_i'} I_i$$



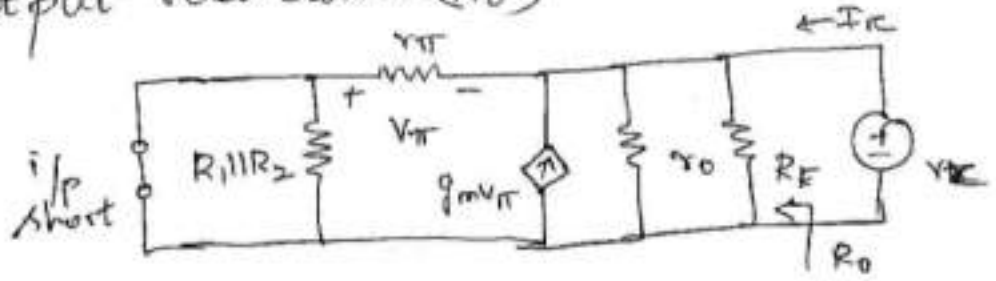
$$\frac{I_b}{I_i} = \frac{R_1 \| R_2}{(R_1 \| R_2) + R_i'} \quad \text{— (3)}$$

$$A_i = \frac{I_e}{I_i} = \frac{I_e}{I_o} \times \frac{I_o}{I_b} \times \frac{I_b}{I_i} = \left(\frac{r_o}{r_o + R_E}\right) \cdot (1+\beta) \left(\frac{R_1 \| R_2}{R_1 \| R_2 + R_i'}\right)$$

If $R_1 \| R_2 >> R_i'$ & $r_o >> R_E$

$$\boxed{A_i = (1+\beta)}$$

Output resistance (R_o)



$V_s = 0$, $R_s = 0$

Apply test voltage V_x to measure I_x.

↓ Test volt

$$R_o = \frac{V_x}{I_x}$$

Apply KVL to outer loop

$$V_\pi = -V_x$$

Apply KCL

$$I_x + g_m V_\pi = \frac{V_x}{r_\pi} + \frac{V_x}{r_o} + \frac{V_x}{R_E}$$

$$I_x - g_m V_x = \frac{V_x}{r_\pi} + \frac{V_x}{r_o} + \frac{V_x}{R_E}$$

$$\frac{I_x}{V_x} = \frac{1}{R_o} = g_m + \frac{1}{r_\pi} + \frac{1}{r_o} + \frac{1}{R_E}$$

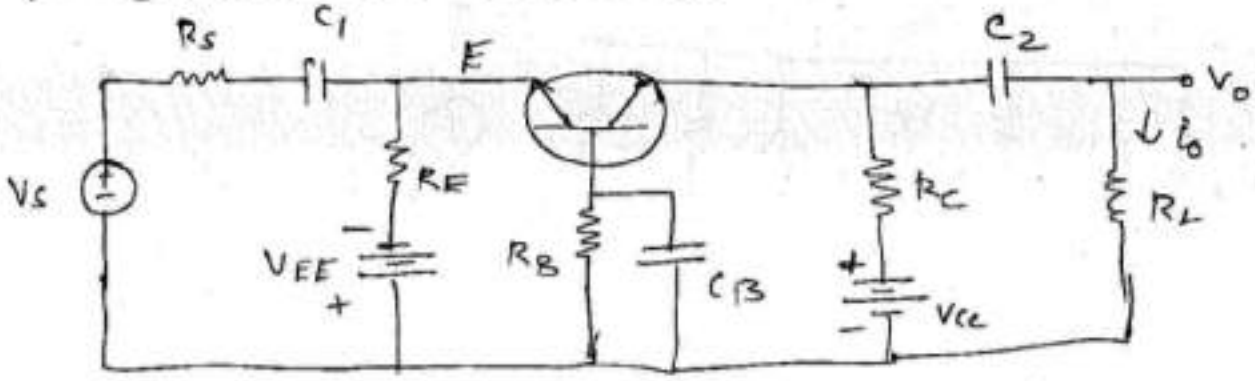
$$R_o = \frac{1}{g_m} \| r_\pi \| r_o \| R_E$$

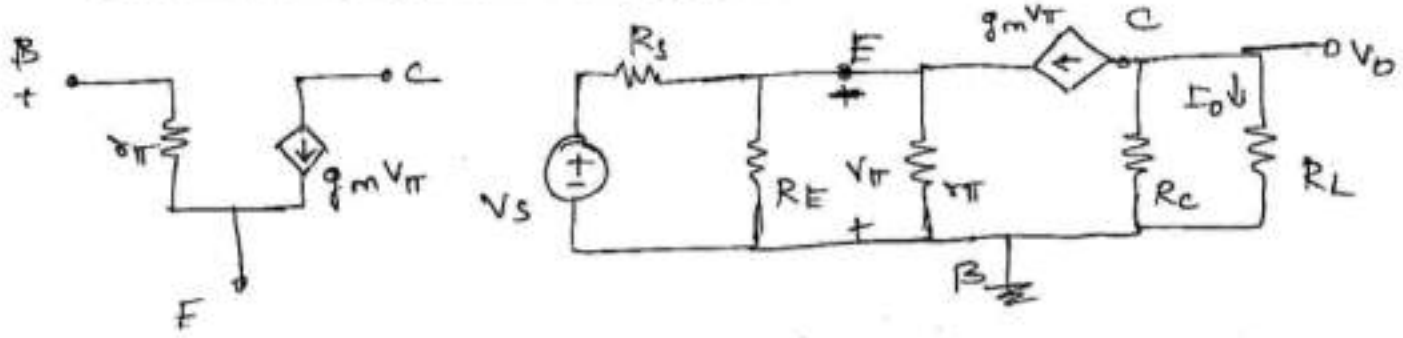
o/p resistance written in

$$\frac{1}{R_o} = \left(g_m + \frac{1}{r_\pi}\right) + \frac{1}{r_o} + \frac{1}{R_E} = \left(\frac{1+\beta}{r_\pi}\right) + \frac{1}{r_o} + \frac{1}{R_E}$$

$$R_o = \frac{r_\pi}{1+\beta} \| r_o \| R_E$$

Common Base Amplifier





Voltage gain :

$$V_o = (-g_m V_\pi)\, R_C \| R_L \qquad \text{——(1)}$$

Apply KCL to emitter node

$$\frac{V_s - (-V_\pi)}{R_S} + \frac{V_\pi}{R_E} + \frac{V_\pi}{r_\pi} + g_m V_\pi = 0 \qquad \text{——(2)}$$

$$V_\pi \left(\frac{1}{R_S} + \frac{1}{R_E} + \frac{1}{r_\pi} + g_m \right) = -\frac{V_s}{R_S} \qquad \text{—(3)}$$

$\left[\because \beta = g_m r_\pi \right]$

$$V_\pi \left(\frac{1}{R_S} + \frac{1}{R_E} + \frac{(1+\beta)}{r_\pi} \right) = \frac{V_s}{R_S} \qquad \text{—(4)}$$

$$V_\pi = \frac{-V_s}{R_S} \left[R_S \| R_E \| \frac{r_\pi}{1+\beta} \right] \qquad \text{——(5)}$$

Sub (5) in (1)

$$V_o = -g_m \left[-\frac{V_s}{R_S} \left[R_S \| R_E \| \frac{r_\pi}{1+\beta} \right] \right] R_C \| R_L$$

$$A_v = \frac{V_o}{V_s} = g_m (R_c \| R_L)$$

Current gain (A_i)

Apply KCL to emitter node

$$I_i + \frac{V_\pi}{R_E} + \frac{V_\pi}{r_\pi} + g_m V_\pi = 0$$

$$V_\pi \left(\frac{1}{R_E} + \frac{1}{r_\pi} + g_m \right) = -I_i$$

$$V_\pi \left[\frac{1}{R_E} + \frac{(1+\beta)}{r_\pi} \right] = -I_i$$

$$V_\pi = -I_i \left[R_E \| \frac{r_\pi}{1+\beta} \right] \quad \text{— (8)}$$

Using current division formula

$$I_o = (-g_m V_\pi) \frac{R_c}{R_c + R_L} \quad \text{— (9)}$$

Sub (8) in (9)

$$I_o = -g_m \left[-I_i \left[R_E \| \frac{r_\pi}{1+\beta} \right] \right] \left[\frac{R_c}{R_c + R_L} \right]$$

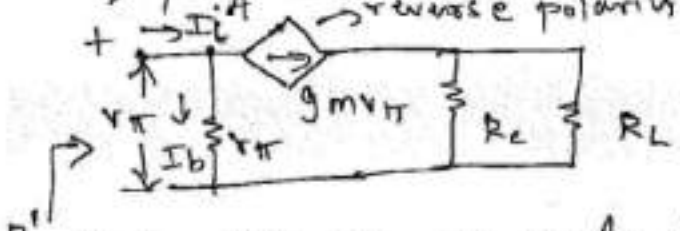
$$A_i = \frac{I_o}{I_i} = \frac{g_m R_c}{R_c + R_L} \left[R_E \| \frac{r_\pi}{1+\beta} \right]$$

$R_E \to \infty \quad R_L \to 0$

$$A_i = \frac{g_m r_\pi}{1+\beta} = \frac{\beta}{1+\beta} = \alpha$$

α – CB current gain of Tr.

Input Resistance



Apply R_{LL} to I/p node A

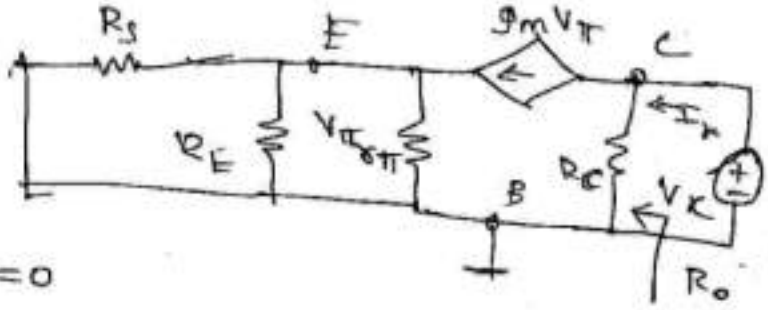
$$I_i = I_b + g_m V_\pi = \frac{V_\pi}{r_\pi} + g_m V_\pi = V_\pi \left(\frac{1 + g_m r_\pi}{r_\pi} \right)$$

$$= V_\pi \frac{(1+\beta)}{r_\pi}$$

$$R_i' = \frac{V_\pi}{I_i} = \frac{r_\pi}{1+\beta} = r_e$$

output Resistance (R_o)

$V_s \rightarrow$ set to 0



$$g_m V_\pi + \frac{V_\pi}{r_\pi} + \frac{V_\pi}{R_E} + \frac{V_\pi}{R_s} = 0$$

$V_\pi = 0$ / $\because g_m V_\pi = 0$

$$\boxed{R_o = R_c}$$

MOSFET AMPLIFIER:

Small Signal Parameters:

The time varying signal source generate a time varying component of the gate to source voltage. The instantaneous gate to source voltage is given by

$$v_{GS} = V_{GSQ} + v_i = V_{GSQ} + v_{gs} \quad \cdots (1)$$

where V_{GSQ} is the dc component and v_{gs} is the ac component.

The instantaneous drain current is

$$i_D = K_n (v_{GS} - V_T)^2 \quad \cdots (2)$$

Now substitute eqn (1) in (2) we get.

$$i_D = K_n \left[(V_{GSQ} + v_{gs}) - V_T \right]^2$$

$$= K_n \left[(V_{GSQ} - V_T) + v_{gs} \right]^2$$

$$\therefore i_D = \underbrace{K_n (V_{GSQ} - V_T)^2}_{\text{DC component}} + \underbrace{K_n v_{gs}^2}_{\text{produces harmonic}} + \underbrace{2 K_n v_{gs} (V_{GSQ} - V_T)}_{\text{Time varying } I_D \text{ component.}} \quad \cdots (3)$$

For a sinusoidal input signal the squared term produces undesirable harmonics or non linear distortion in the output voltage. To minimize these harmonics we must have

$$v_{gs} \ll 2(V_{GSQ} - V_T) \quad \cdots (4)$$

The above condition represent the small signa condition that must be satisfied for linear applic

Neglecting the v_{gs}^2 term we can write above relation as

$$i_D = I_{DQ} + i_d \quad \text{--- (4)}$$

where as $$I_{DQ} = K_n (V_{GSQ} - V_T)^2 \quad \text{--- (5)}$$

$$i_d = 2K_n (V_{GSQ} - V_T) v_{gs} \quad \text{--- (6)}$$

The Small Signal drain current is related to the small signal gate to Source voltage by the transco-ductance g_m.

$$\therefore g_m = \frac{I_d}{v_{gs}} = \frac{2K_n (V_{GSQ} - V_T) \cancel{v_{gs}}}{\cancel{v_{gs}}}$$

$$\boxed{\therefore g_m = 2K_n (V_{GSQ} - V_T)} \quad \text{--- (7)}$$

The transconductance is a ratio of output current to input voltage and hence it represents the gain of the MOSFET.

Small Signal Equivalent Circuit.

The Small Signal low frequency ac equivalent circuit for n-channel MOSFET is shown in fig.

The relation of I_d by v_{gs} is included as a current source $g_m v_{gs}$ connected from drain to source.

The input impedance is represented.

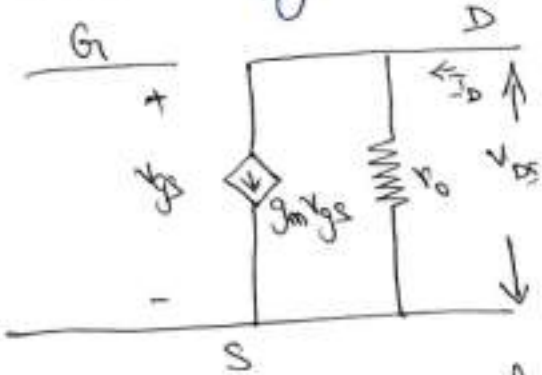


fig. Expanded Small Signal equivalent circuit including output resistance

by the open circuit as its input terminals, since gate current I_G is zero.

We know that the circuit has the finite output resistance of a MOSFET biased in the saturation region because of the nonzero slope in the i_D versus v_{DS} curve. We know that:

$$i_D = k_n \left[(v_{GS} - V_T)^2 (1 + \lambda v_{DS}) \right] \quad \ldots (8)$$

where λ is the channel length modulation.

The small signal output resistance is given by.

$$r_o = \left[\frac{\partial i_D}{\partial v_{DS}} \right]^{-1} \Bigg|_{v_{GS} = V_{GSQ} = \text{Constant}}$$

Now differentiate equation (8) w.r.t v_{DS} we get.

$$r_o = \left[\lambda k_n (V_{GSQ} - V_T)^2 \right]^{-1}$$

$$\therefore r_o \approx \left[\lambda I_{DQ} \right]^{-1} \quad \ldots (9)$$

The above equation shows that the small signal output resistance is a function of Q-point parameters.

Common Source Amplifier:

The Common Source circuit with voltage divider biasing and coupling capacitors. The MOSFET is biased near the middle of the saturation region by R_1 and R_2 resistors to work as an amplifier. The signal frequency is sufficiently large for the coupling capacitors to act essentially as a short circuit. The resistance R_{si} is the source resistance of the signal voltage source V_i.

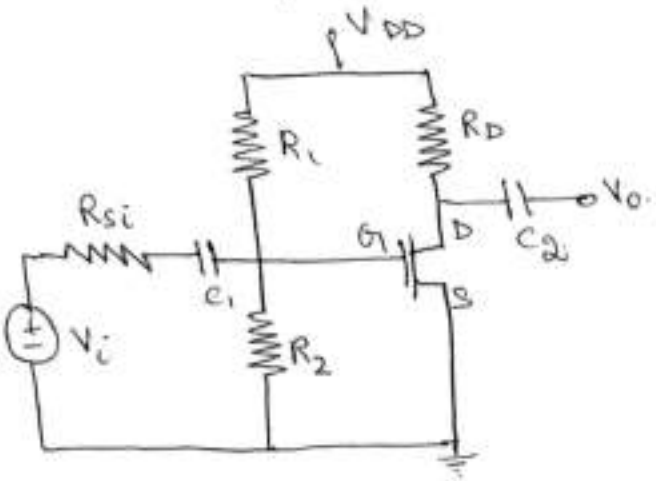


fig. Common Source with Voltage divider Bias

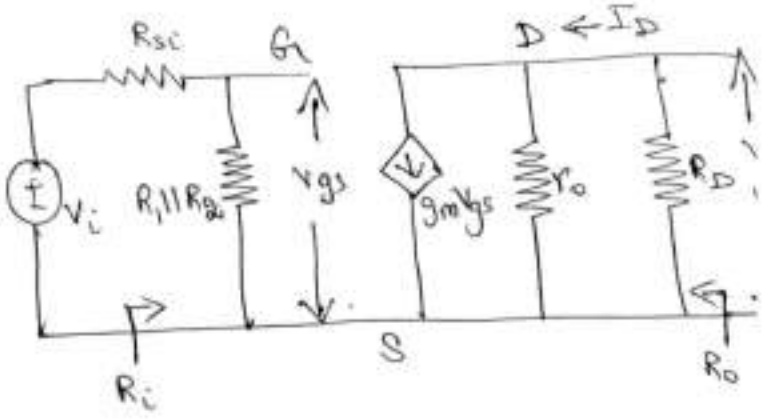


fig. Small Signal equivalent circuit.

Input Resistance:- (R_i)

From the Small Signal equivalent circuit we can write

$$R_i = R_1 \| R_2 \quad \text{---} \quad (1)$$

output Resistance :- (R_o)

$$R_o = R_D \| r_o \quad \text{---} \quad (2)$$

Voltage Gain: (A_v)

The output voltage can be written as

$$V_o = -g_m V_{gs} (r_o \| R_D) \quad \text{---} \quad (3)$$

Using voltage divider rule, the input gate to source voltage is written as

$$V_{gs} = \left[\frac{R_i}{R_i + R_{si}}\right] V_i \quad \cdots (4)$$

Now substitute equ (4) in (3) we get.

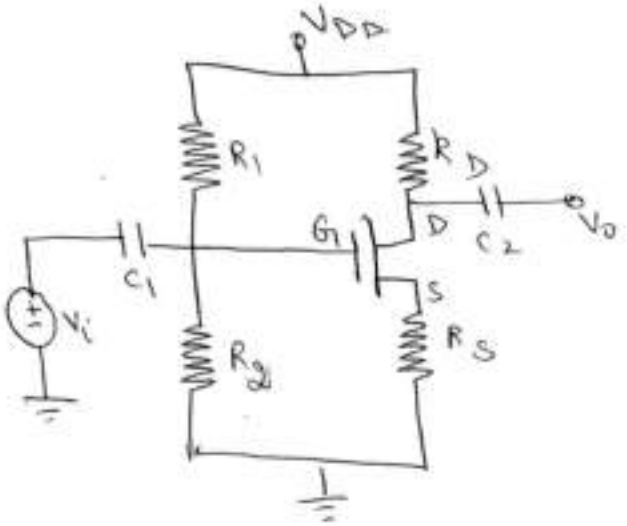
$$V_o = -g_m \left[\frac{R_i}{R_i + R_{si}}\right] V_i \, (r_o \| R_D)$$

$$\therefore A_v = \frac{V_o}{V_i} = -g_m (r_o \| R_D) \left[\frac{R_i}{R_i + R_{si}}\right] \quad \cdots (5)$$

Since R_{si} is not zero, the amplifier input signal V_{gs} is less than the signal voltage. This is known as loading effect. It reduces the voltage gain of the amplifier.

Common source amplifier with source resistance :-

The common source amplifier with source resistance is shown below. The source resistor is introduced to stabilize the Q point against variation in the MOSFET parameter.



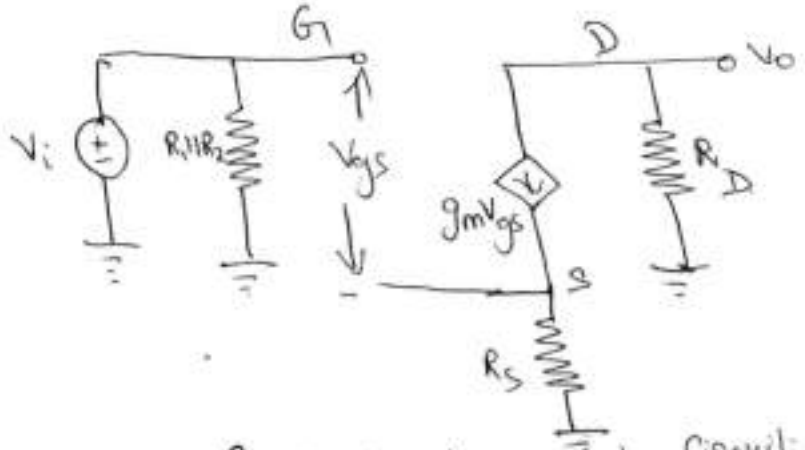


fig. Small signal equivalent circuit of common source with source resistor.

From the small signal equivalent circuit we can write.

$$V_o = -g_m V_{gs} R_D \quad \cdots (1)$$

Apply KVL between input to gate - source loop we can write

$$V_i = V_{gs} + g_m V_{gs} R_S$$

$$V_i = V_{gs} [1 + g_m R_S] \quad \cdots (2)$$

$$\therefore V_{gs} = \frac{V_i}{[1 + g_m R_S]} \quad \cdots (3)$$

Substitute equation (3) in (1) we can write.

$$V_o = \frac{-g_m V_i R_D}{[1 + g_m R_S]}$$

$$\therefore A_v = \frac{V_o}{V_i} = \frac{-g_m R_D}{[1 + g_m R_S]} \quad \cdots (4)$$

Common source circuit with source bypass Capacitor

A Source bypass capacitor connected across the Source resistor in the common-source circuit will minimize the loss in the small signal voltage gain while maintaining Q-point stability.

We can further increase the Q-point stability replacing the source resistor with a constant current Source.

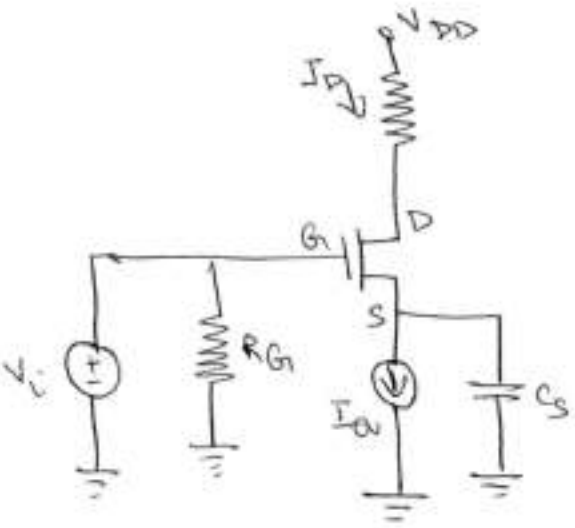


Fig. Common Source Circuit with Source bypass capacitor.

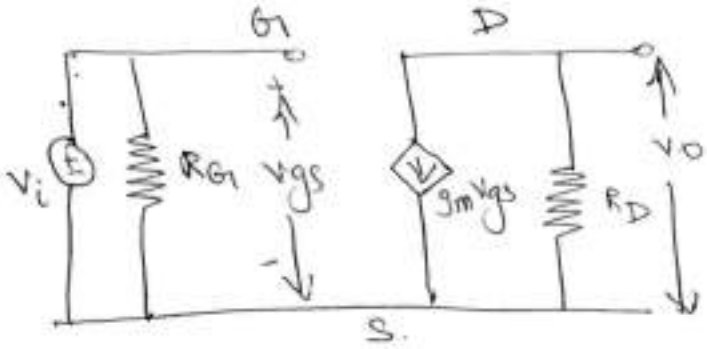


Fig. Small Signal equivalent circuit.

From the small signal equivalent circuit we can write.

Input Resistance (R_i):

$$R_i = R_G$$

Output Resistance (R_o):

$$R_o = R_D$$

Voltage Gain (A_v):-

The output voltage can be written as

$$V_o = -g_m V_{gs} R_D$$

From the Small signal equivalent circuit.

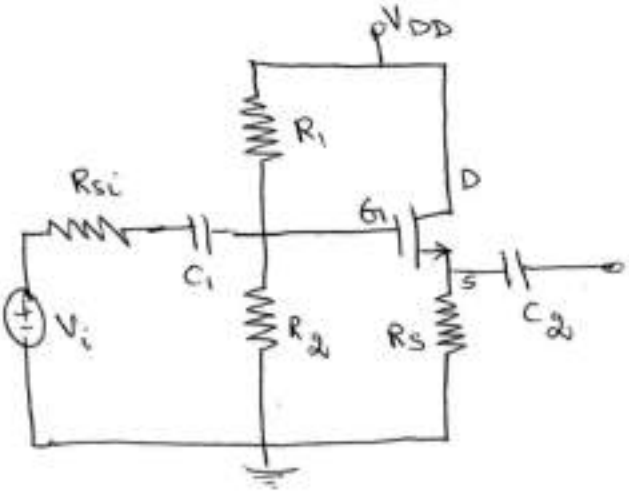
$$V_i = V_{gs}$$

$$\therefore V_o = -g_m V_i R_D$$

$$\text{ie } A_v = \frac{V_o}{V_i} = -g_m R_D$$

MOSFET Source Follower Amplifier :-

In source follower amplifier circuit, output is taken from the source with respect to ground and drain is connected directly to V_{DD}. The small signal equivalent circuit of source follower is shown below.



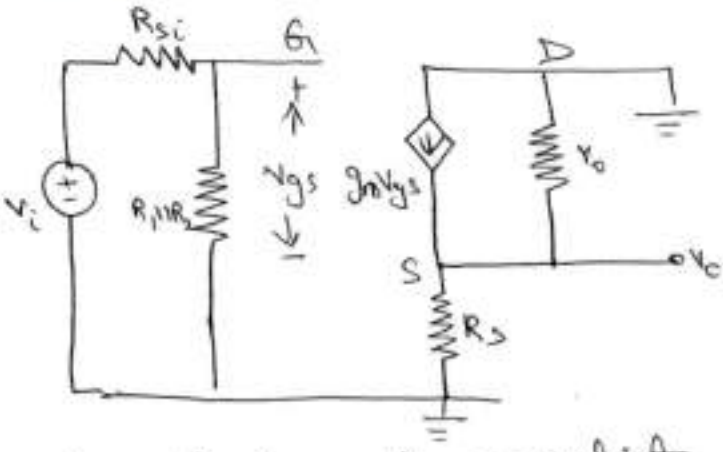


fig. Small signal equivalent circuit.

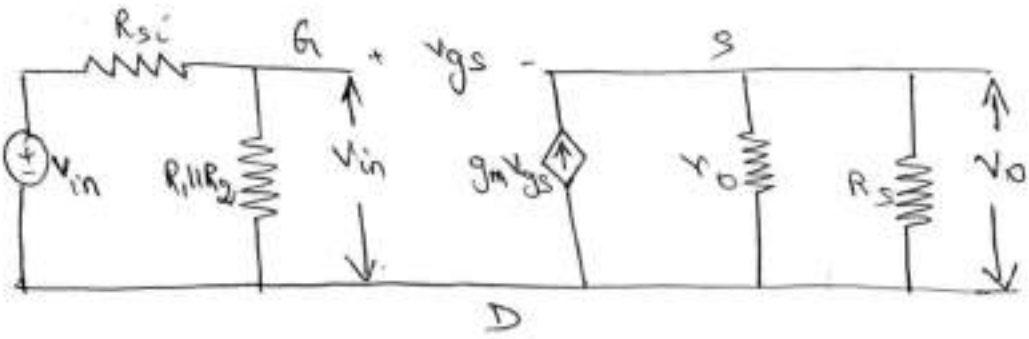


fig. Simplified small signal equivalent circuit of Common Drain.

Input Resistance (R_i) :-

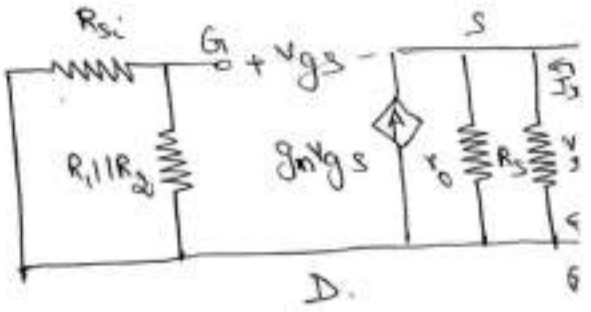
From the small signal equivalent circuit

$$R_i = R_1 \| R_2 \quad \text{---} \quad (1)$$

Output resistance (R_o) :-

To calculate the output resistance we set all independent small signal source equal to zero by shorting them apply the test voltage to output terminals and

measure the test current.



Apply KCL to the o/p node we can write.

$$I_x = \frac{V_x}{r_o} + \frac{V_x}{R_S} - g_m V_{gs} \quad \cdots (2)$$

Since input current is zero we have

$$V_{gs} = -V_x \quad \cdots (3)$$

$$\therefore I_x = \frac{V_x}{r_o} + \frac{V_x}{R_S} + g_m V_x$$

$$I_x = V_x \left[\frac{1}{r_o} + \frac{1}{R_S} + g_m \right]$$

$$\therefore R_o = \frac{V_x}{I_x} = \frac{1}{\left[\frac{1}{r_o} + \frac{1}{R_S} + g_m \right]}$$

$$\therefore R_o = r_o \| R_S \| \frac{1}{g_m} \quad \cdots (4)$$

Voltage Gain (A_v):-

From the small signal equivalent circuit the output ~~over~~ voltage can be written as

$$V_o = g_m V_{gs} (r_o \| R_S) \quad \cdots (5)$$

Apply KVL to the output loop.

$$V_{in} = V_{gs} + V_o \quad \cdots (6)$$

Substitute eqn (5) in (6) we get.

$$V_{in} = V_{gs} + g_m V_{gs} (r_o \| R_S)$$

$$= V_{gs} \left[1 + g_m (r_o \| R_S) \right]$$

$$\therefore V_{gs} = \frac{V_{in}}{\left[1 + g_m (r_o \| R_S) \right]} \quad \cdots (7)$$

Apply voltage divider rule at input

$$V_{in} = \left[\frac{R_i}{R_i + R_{si}}\right] V_i \quad \cdots (8)$$

Now substitute equ (8) in (7) we get.

$$V_{gs} = \frac{1}{1 + g_m(r_o \| R_s)} \left[\frac{R_i}{R_i + R_{si}}\right] V_{in} \quad \cdots (9)$$

Substitute equation (9) in (5) we can write

$$\therefore V_o = \frac{g_m(r_o \| R_s)}{1 + g_m(r_o \| R_s)} \left[\frac{R_i}{R_i + R_{si}}\right] V_{in}$$

$$\therefore A_v = \frac{V_o}{V_{in}} = \frac{g_m(r_o \| R_s)}{1 + g_m(r_o \| R_s)} \left[\frac{R_i}{R_i + R_{si}}\right] \quad \cdots (10)$$

MOSFET Common Gate Amplifier :-

The circuit diagram of common gate amplifier circuit is shown below. Here constant current source I_a is used to bias the MOSFET. The resistor R_G at the gate prevents the build up of static charge on the gate terminals and the bypass capacitor C_G ensure that the gate is at signal ground.

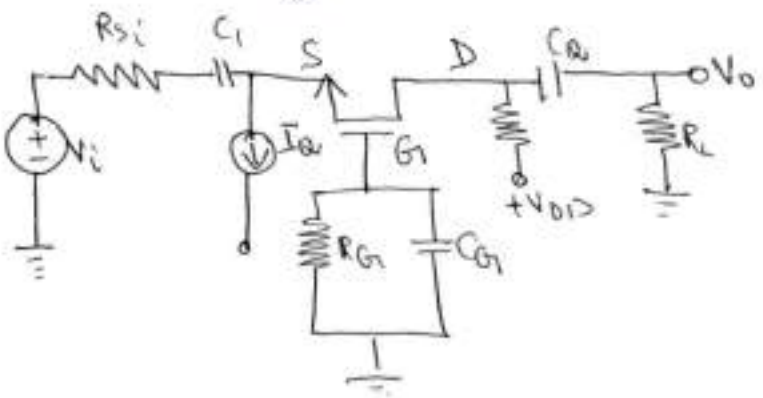


Fig. Common gate Amplifier

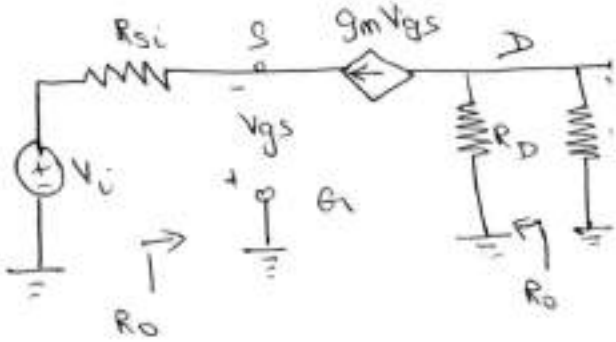


Fig. Small signal equivalent circuit.

The Coupling Capacitor C_1 Couples the signal to the Source terminal and coupling Capacitor C_2 Couples the Output Voltage to the load resistor R_L

Input resistance : (R_i)

From the Small Signal equivalent circuit we Can write

$$R_i = \frac{-V_{gs}}{I_i} \quad \cdots (1)$$

where as $I_i = -g_m V_{gs}$ (Both are in opposite direct

$$\therefore R_i = \frac{-V_{gs}}{-g_m V_{gs}} = 1/g_m \quad \cdots (2)$$

Output Resistance : (R_o)

when input sourse voltage is zero, then the output resistance looking back from the load resistance is given by.

$$R_o = R_D \quad \cdots (3)$$

Voltage Grain (A_v) :

The output voltage V_o Can be written as

$$V_o = -g_m V_{gs} (R_D \| R_L) \quad \cdots (4)$$

Apply KVL to input side we Can write.

$$V_i = I_i R_{si} - V_{gs} \quad \cdots (5)$$

Substitute I_i in eqn (5)

$$V_i = -g_m V_{gs} R_{si} - V_{gs}$$

$$= -V_{gs} [g_m R_{si} + 1]$$

$$V_{gs} = \frac{-V_i}{[1+g_m R_{si}]} \quad \cdots (6)$$

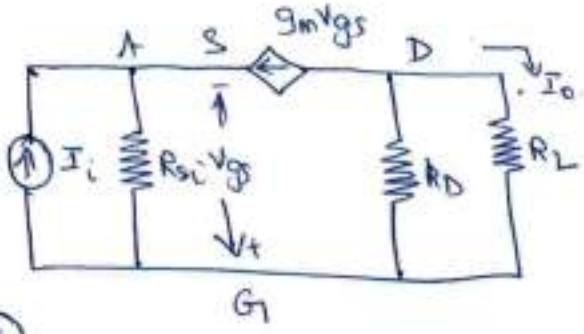
Substitute V_{gs} in equ (4) we get.

$$V_o = -g_m \left[\frac{-V_i}{1+g_m R_{si}}\right] (R_D \| R_L)$$

$$\therefore A_v = \frac{V_o}{V_i} = \frac{g_m (R_D \| R_L)}{[1+g_m R_{si}]} \quad \cdots (7)$$

Current gain (A_I) :-

The signal input to the common gate amplifier may be current.



Apply current divider rule at the

$$I_o = (-g_m V_{gs}) \left[\frac{R_D}{R_D + R_L}\right] \quad \cdots (8)$$

Apply KCL at node A we have.

$$I_i + \frac{V_{gs}}{R_{si}} \quad I_i = -\frac{V_{gs}}{R_{si}} - g_m V_{gs}$$

$$\therefore I_i = -V_{gs}\left[\frac{1+g_m R_{si}}{R_{si}}\right]$$

$$V_{gs} = -\frac{I_i R_{si}}{(1+g_m R_{si})} \quad \cdots (9)$$

Now Substitute equ (9) in (8) we get.

$$I_o = (-g_m)\left(\frac{-I_i R_{si}}{1+g_m R_{si}}\right)\left(\frac{R_D}{R_D + R_L}\right)$$

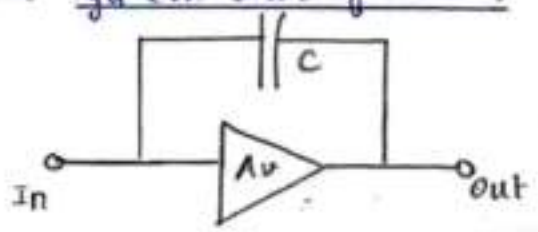
$$\therefore A_I = \frac{I_o}{I_i} = \frac{g_m R_{si}}{(1+g_m R_{si})}\left(\frac{R_D}{R_D + R_L}\right) \quad \cdots (10).$$

At higher frequencies, the reactances of the junction capacit are low. As frequencies increase, the reactances of the junction capacitances fall. when these reactances becomes small enough, they provide shunting effect as they are in parallel with junctions. This reduces the circuit gain and hence the output voltage.

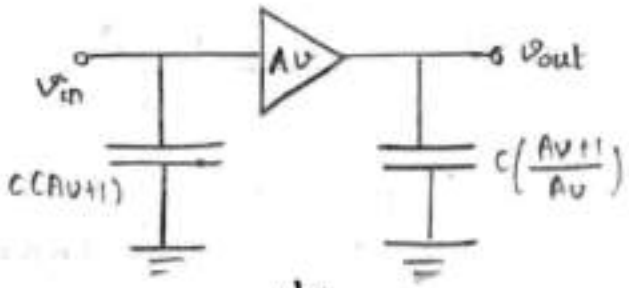
4.2.44. HILLER THEOREM:

For the analysis purpose, in transistor amplifiers, it is necessary to split the capacitance between input and the output. This can be achieved by Hiller's Theor as shown in fig.

Av represents absolute voltage gain of the amplifier at midrange frequencies and C represents Either C_{bc} (in case of and C_{gd} (in case of JFET).



(a)



(b)

SPLITTING OF CAPACITORS USING HILLER'S THEOR

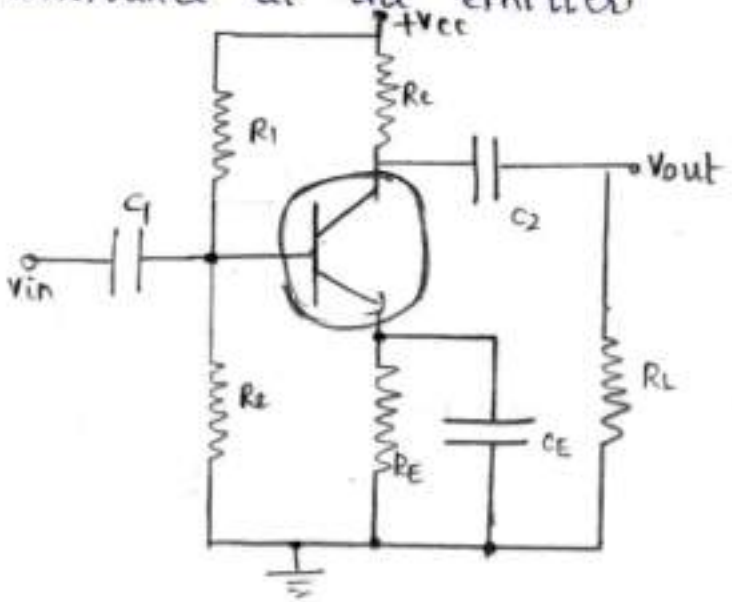
4.3. BJT FREQUENCY RESPONSE:

Generally, BJT Frequency response involves the low frequency response of BJT. Let us consider a typical common emitter amplifier, as shown in fig.

The amplifier shown in fig. has three RC networks that affects its gain as the frequency is reduced below

There are:

1. RC network formed by the input coupling capacitor and the input impedence of the amplifier.
2. RC network formed by the output coupling capacitor the resistance at the collector and the load resistance
3. RC network formed by the emitter bypass capacitor and the resistance at the emitter.



TYPICAL RC COUPLED CE AMPLIFIER

1. INPUT RC NETWORK:

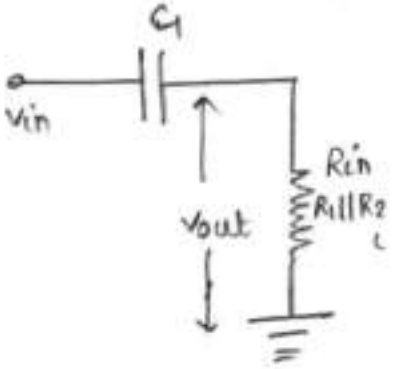


Fig. shows the input RC network formed by C_1 and the input impedence of the amplifier. Note that Vout shown in fig. is the output voltage of the network.

Applying voltage divider theorem,

$$V_{out} = \left[\frac{R_{in}}{\sqrt{R_{in}^2 + X_{C_1}^2}} \right] V_{in}$$

We know that the critical point in the amplifier response is generally accepted to occur when the output voltage is 70.7 percent of the input ($V_{out} = 0.707 V_{in}$). Thus, we can write, at critical point,

$$\frac{R_{in}}{\sqrt{R_{in}^2 + X_{C_1}^2}} = 0.707 = \frac{1}{\sqrt{2}}$$

∴ At this condition, $R_{in} = X_{C_1}$

The overall gain is reduced due to the attenuation provide by the input RC network. The reduction in overall gain is given by

$$A_v = 20 \log \left(\frac{V_{out}}{V_{in}}\right) = 20 \log (0.707)$$

$$= -3\,dB$$

The frequency f_c at this condition is called lower critic frequency and is given by

$$f_c = \frac{1}{2\pi R_{in} C_1}$$ where $R_{in} = R_1 || R_e || R_{in(base)}$,

$R_{in(base)} = h_{ie}$.

$$\therefore f_c = \frac{1}{2\pi (R_1 || R_2 || h_{ie}) C_1}$$

If the resistance of the input source is taken into accou the above equation becomes,

$$f_c = \frac{1}{2\pi (R_s + R_{in}) C_1}$$

The phase angle in an input RC network is expressed a

$$\theta = \tan^{-1} \left(\frac{X_{C_1}}{R_{in}}\right)$$

2. OUTPUT RC NETWORK:

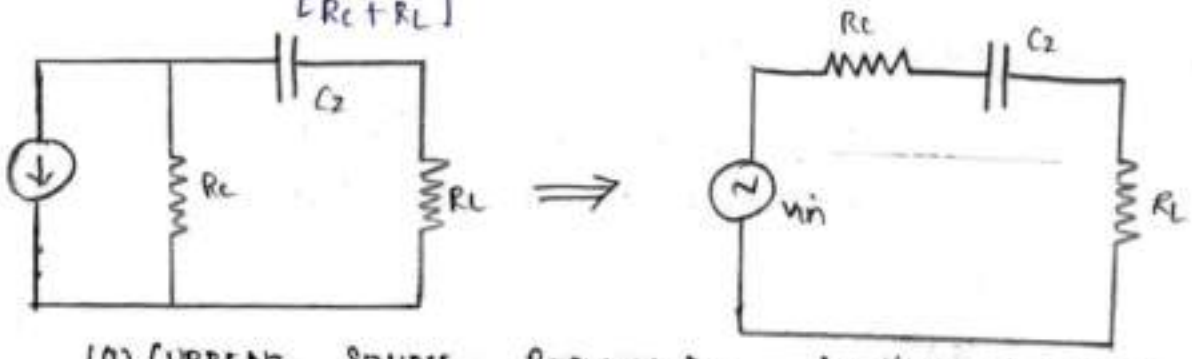
Fig. shows output RC network formed by C_2, resistance at the collector and the load resistance.

The critical frequency for this RC network is given by

$$f_c = \frac{1}{2\pi (R_C + R_L) C_2}$$

The phase angle in the output RC network is given by

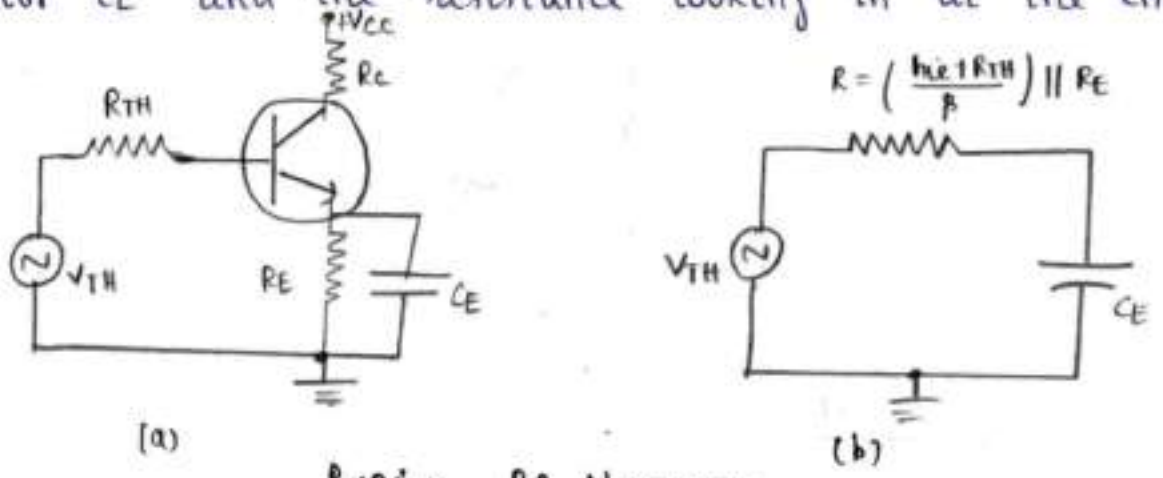
$$\theta = \tan^{-1}\left[\frac{X_{C2}}{R_C + R_L}\right]$$



(a) CURRENT SOURCE REPLACED BY (b) VOLTAGE SOURCE

3. BYPASS NETWORK:

Fig. shows RC network formed by the emitter bypass capacitor CE and the resistance looking in at the emitter.



(a) (b)

BYPASS RC NETWORK

Here, $\frac{R_{TH} + h_{ie}}{\beta}$ is the resistance at the emitter. It is derived as follows:

$$R = \frac{V_c}{I_c} + \frac{h_{ie}}{\beta} \simeq \frac{V_b}{\beta I_b} + \frac{h_{ie}}{\beta}$$

$$= \frac{I_b R_{TH}}{\beta I_b} + \frac{h_{ie}}{\beta} \simeq \frac{R_{TH} + h_{ie}}{\beta}$$

where $R_{TH} = R_1 || R_2 || R_s$.

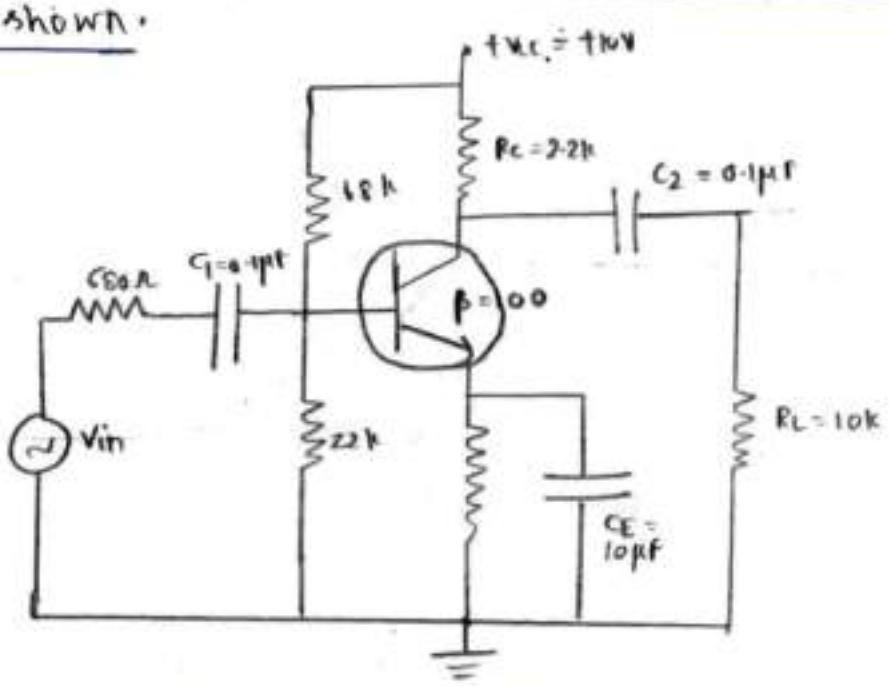
The critical frequency at the bypass network is given by

$$f_c = \frac{1}{2\pi R C_E} = \frac{1}{2\pi \left(\frac{R_{TH} + h_{ie}}{\beta} || R_E\right) C_E}$$

Each network has its own critical frequency. It is not necessary all frequencies should be equal. The highest critical frequency is

Ex: PROBLEMS:-

4.3.1. Determine the low frequency response of the amplifier circuit shown.



Soln: It is necessary to analyse each network to determine the critical frequency of the amplifier.

(a) Input RC network:

$$f_{c(input)} = \frac{1}{2\pi [R_s + (R_1 \| R_2 \| h_{ie})] C_1}$$

$$= \frac{1}{2\pi [680 + (68K \| 22K \| 1.1K)] \times 0.1 \times 10^{-6}}$$

$$= \frac{1}{2\pi [680 + 1031.7] \times 0.1 \times 10^{-6}}$$

$$f_{c(input)} = 929.8 Hz$$

(b) Output RC network:

$$f_{c(output)} = \frac{1}{2\pi (R_c + R_L) C_2}$$

$$= \frac{1}{2\pi (2.2K + 10K) \times 0.1 \times 10^{-6}}$$

$$f_{c(output)} = 130.45 Hz$$

(c) Bypass RC network :

$$f_{c(bypass)} = \frac{1}{2\pi\left[\frac{R_{TH} + h_{ie}}{\beta} \,||\, R_E\right] C_E}$$

$$= \frac{1}{2\pi\left[\frac{(R_1 || R_2 || R_S) + h_{ie}}{\beta} \,||\, R_E\right] C_E}$$

$$R_{TH} = 68K \,||\, 22K \,||\, 680$$

$$= 653.28\ \Omega$$

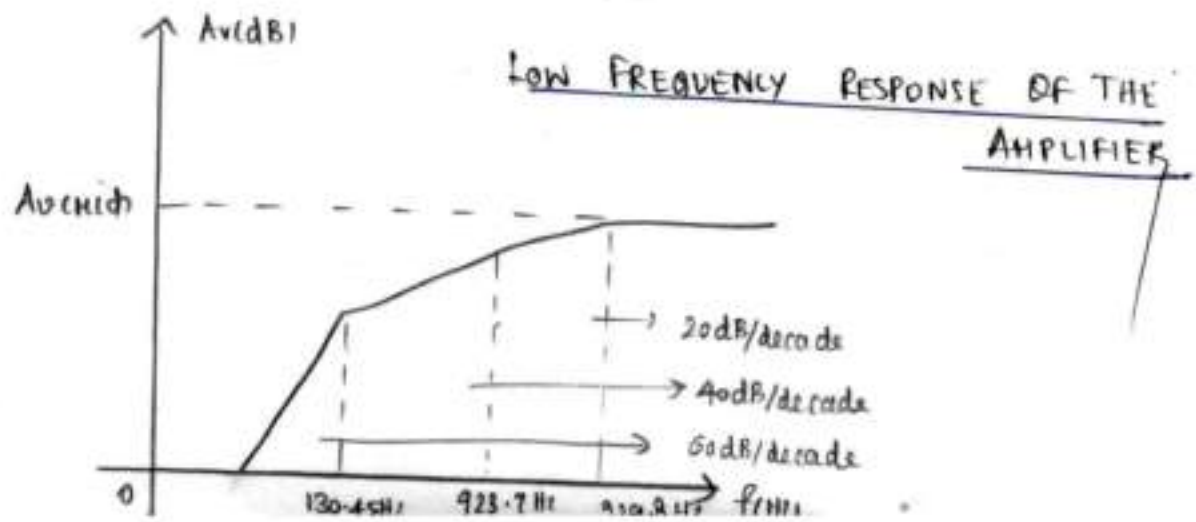
$$f_{c(bypass)} = \frac{1}{2\pi\left[\frac{653.28 + 1100}{100} \,||\, 1k\right] \times 10 \times 10^{-6}} \quad \because h_{ie} = 1.1k\Omega$$

$$= \frac{1}{2\pi\,[17.23] \times 10 \times 10^{-6}}$$

$$f_{c(bypass)} = 923.7\,Hz$$

$\therefore$ $f_{c(input)} = 929.8Hz$
$f_{c(output)} = 130.45Hz$
$f_{c(bypass)} = 923.7Hz$

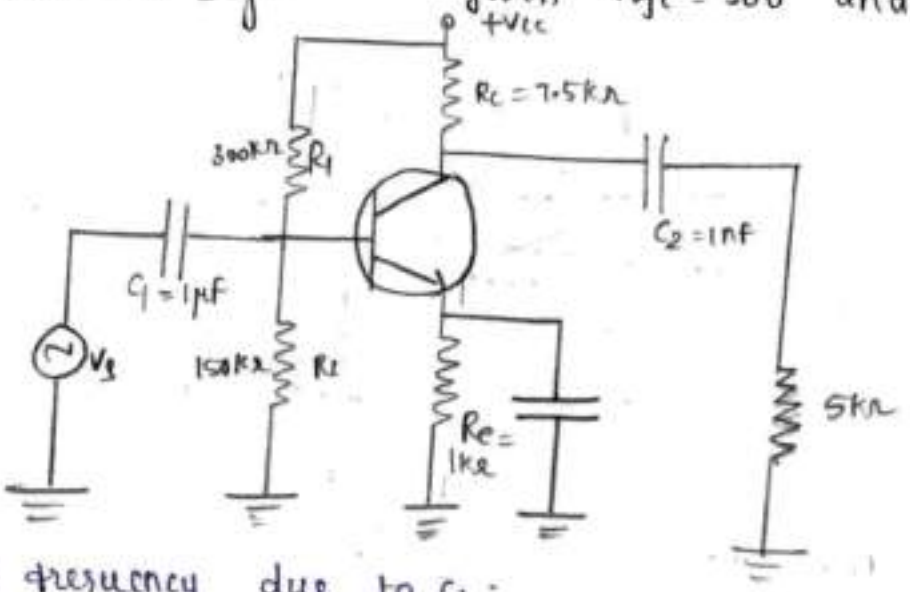
From these equations, it is observed that input network produces the dominant lower critical frequency. The frequency response of the amplifier is drawn as



LOW FREQUENCY RESPONSE OF THE AMPLIFIER

PROBLEMS:-

Ex.4.32 Calculate the cut-off frequencies due to C_1 and C_2 in the circuit shown in fig. given $h_{fe} = 300$ and $h_{ie} = 32k$.



Soln: (a) Cut-off frequency due to C_1:

$$f_c = \frac{1}{2\pi R_{in} C_1} \quad \text{where} \quad R_{in} = R_1 \| R_2 \| h_{ie}$$

$$R_{in} = 300k \| 150k \| 32k$$

$$= \frac{1}{2\pi (300k \| 150k \| 32k) \times 1 \times 10^{-6}}$$

$$f_c = 6.565\,Hz$$

(b) Cut-off frequency due to C_2:

$$f_c = \frac{1}{2\pi (R_c + R_L) C_2}$$

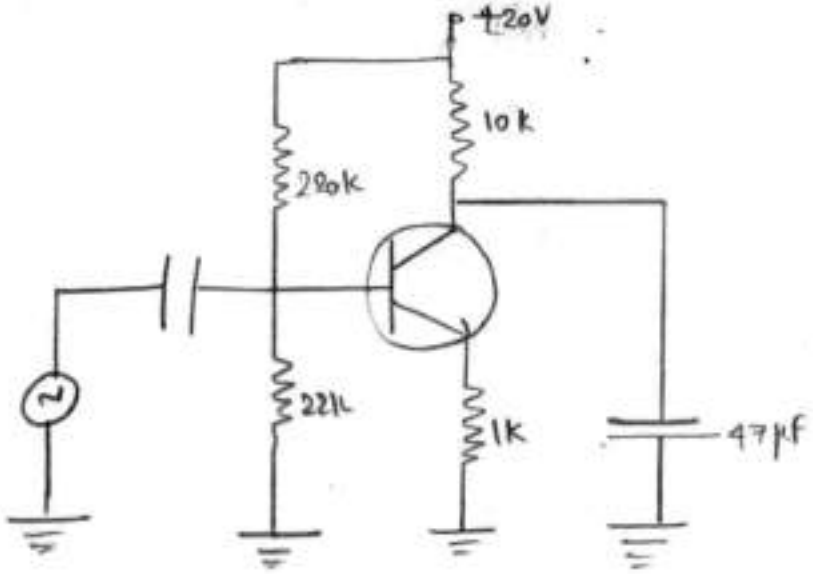
$$= \frac{1}{2\pi (7.5 \times 10^3 + 5 \times 10^3) \times 1 \times 10^{-7}}$$

$$f_c = 12732.4\,Hz$$

Ex.4.33. Determine the cut-off frequency due to the bypass capacitor in the fig.

Given: $h_{ie} = 1k$

$h_{fe} = 200$



Soln:

$$f_{c(bypass)} = \frac{1}{2\pi\left[\frac{R_{TH}+h_{ie}}{\beta} \,||\, R_E\right] C_E}$$

$$R_{TH} = R_1 || R_2 || R_3$$

$$= 220k || 22k || 0$$

$$R_{TH} = 0$$

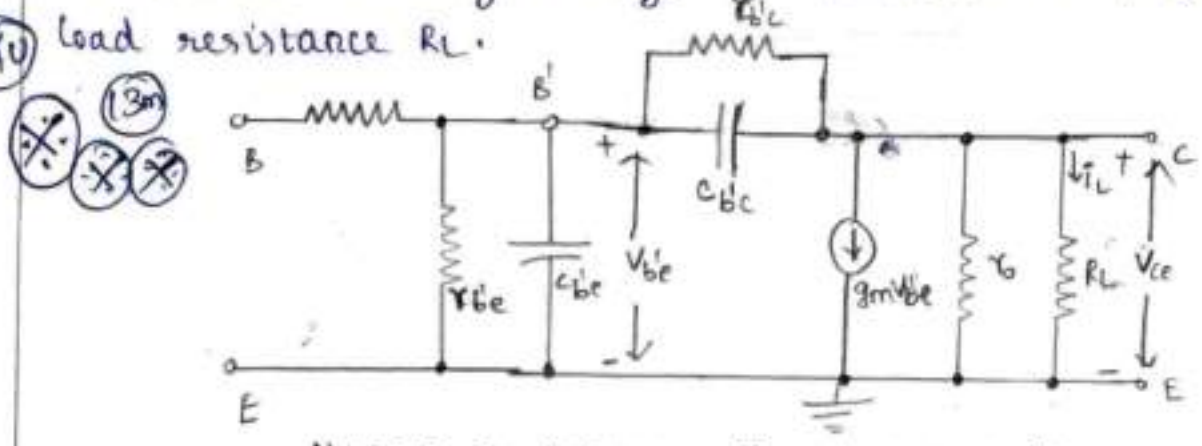
$$f_{c(bypass)} = \frac{1}{2\pi\left[\frac{1000}{200} \,||\, 1\times10^{3}\right] \times 47 \times 10^{-6}}$$

$$= \frac{1}{2\pi\,[4.97] \times 47 \times 10^{-6}}$$

$f_{c(bypass)} = 681Hz$

4.4 CE SHORT CIRCUIT CURRENT GAIN USING HYBRID-π MODEL

Consider a single stage CE transistor amplifier with load resistance R_L.



HYBRID-π CIRCUIT FOR A SINGLE TRANSISTOR WITH R_L.

where, $C_{HO} = \left(1 - \frac{1}{A_V}\right) C_f$. is the Hiller output capacitance

In general, $A_V >> 1$, then the above equation reduces to

$$C_{HO} \simeq C_f$$

The miller effect occurs only in the circuit where there is a 180° phase shift between the input and the output.

4.7. FREQUENCY RESPONSE OF FET :

The drain current of FET is a function of drain to source voltage (V_{DS}) and gate to source voltage (V_{GS}). The linear small signal equivalent circuit for FET can be drawn analogous to the circuit. The input impedence of the FET amplifier is very high. So consider that gate current $I_G = 0$

Assuming varying currents and voltages for a FET

$$i_D = f(V_{GS}, V_{DS})$$

If both drain and gate voltages are varied, the change in drain current is given approximately by first term in the Taylor series expansion of equation.

$\Delta i_d = i_d$; $\Delta V_{GS} = V_{gs}$ and $\Delta V_{DS} = V_{ds}$ for small signal

$$\Delta i_D = \left(\frac{\partial i_D}{\partial V_{gs}}\right)_{V_{DS}} \Delta V_{GS} + \left(\frac{\partial i_D}{\partial V_{DS}}\right)_{V_{GS}} \Delta V_{DS}$$

The small signal notation as for BJT,

$$i_d = g_m V_{gs} + \frac{1}{r_d} V_{ds} \longrightarrow (1)$$

where g_m is the transconductance (or Mutual conductance of the FET.

$$g_m = \left(\frac{\partial i_D}{\partial V_{GS}}\right)_{V_{DS}} \simeq \left(\frac{\Delta i_D}{\Delta V_{GS}}\right)_{V_{DS}} = \left(\frac{i_d}{v_{gs}}\right)_{V_{DS}}$$

Drain ion output resistance of the FET is given as

$$r_d = \left(\frac{\partial V_{DS}}{\partial i_D}\right)_{V_{GS}} \simeq \left(\frac{\Delta V_{DS}}{\Delta i_D}\right)_{V_{GS}} = \left(\frac{v_{ds}}{i_D}\right)_{V_{GS}}$$

Reciprocal of r_d is the drain conductance g_d

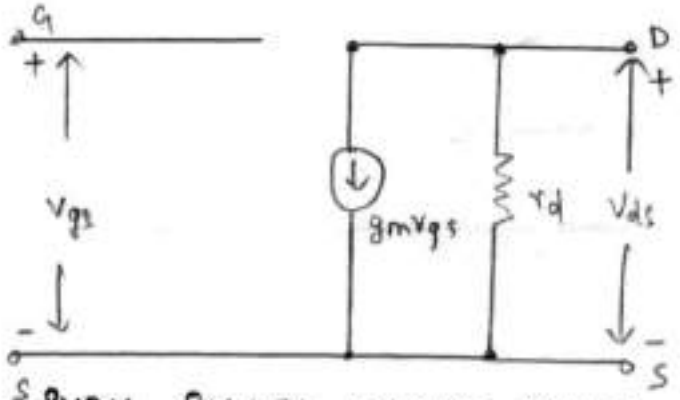
Amplification factor 'μ' for FET may be defined as

$$\mu = \left(\frac{-\partial V_{DS}}{\partial V_{GS}}\right)_{I_D} \simeq \left(\frac{\Delta V_{DS}}{\Delta V_{GS}}\right)_{I_D} = \left(-\frac{v_{ds}}{v_{gs}}\right)_{i_d = 0}$$

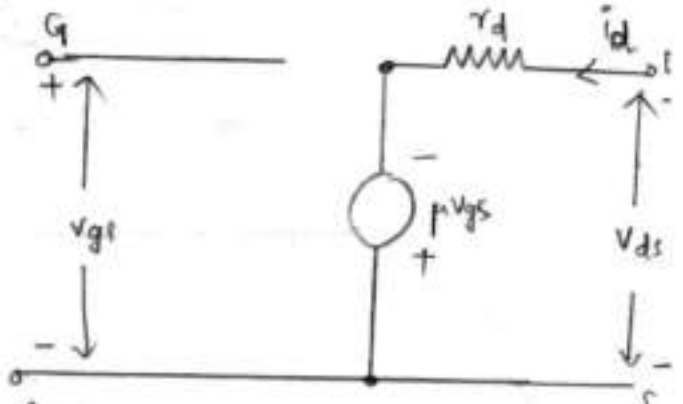
Substitute $i_d = 0$ in eqn (1), we get the relation between μ, g_m & r_d.

$$\mu = g_m r_d$$

A small signal model for FET in common source configuration can be drawn by using equation (1),



SMALL SIGNAL CURRENT SOURCE MODEL FOR FET IN CS CONFIGURATION



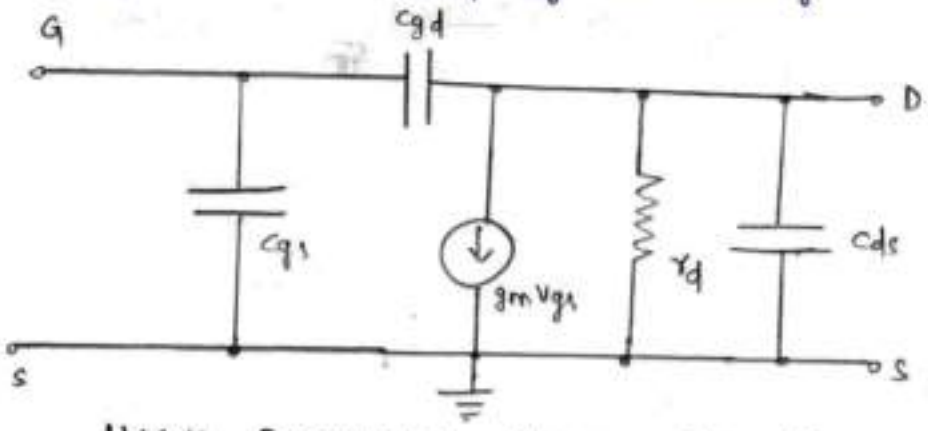
SMALL SIGNAL VOLTAGE SOURCE MODEL FOR FET IN CS CONFIGU

NOTE:

The input resistance between the gate and source is infinite, since it is assumed that the reverse biased gate draws no current.

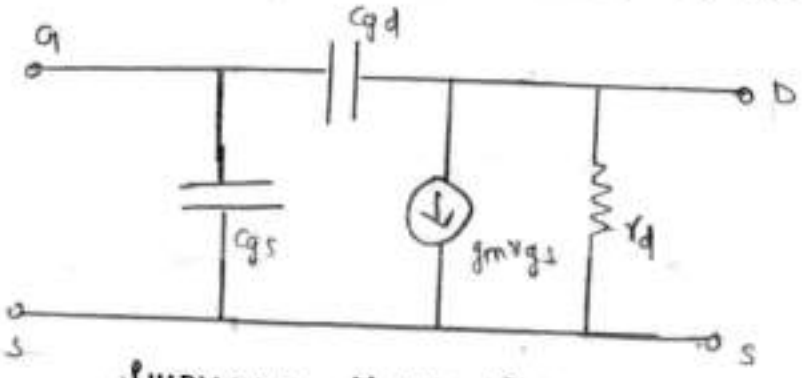
4.8. HIGH FREQUENCY ANALYSIS OF CS MOSFET AMPLIFIERS:

Fig. shows the high frequency equivalent circuit model for MOSFET. In this model, the capacitance C_{ds} can be neglected to simplify the analysis.



HIGH FREQUENCY MODEL OF FET

- In the high frequency model of FET, the capacitances between nodes have to be added in the low frequency mod
- The resultant equivalent circuit is shown in Fig.



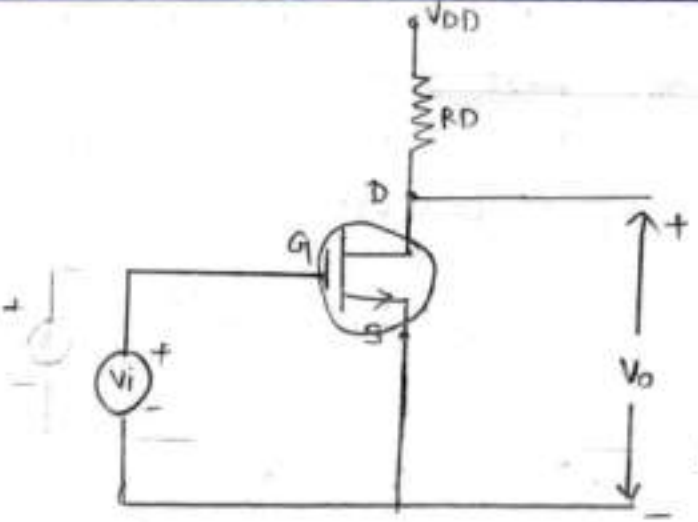
SIMPLIFIED HIGH FREQUENCY MODEL OF FET

- C_{gs} represents the barrier capacitance between gate a source
- C_{gd} represents the barrier capacitance between gate an drain.
- C_{ds} represents the drain to source capacitance of the cha
- The internal capacitances lead to feedback from output to input and the voltage amplification decreases at highe frequencies.

$$\omega_T = \frac{g_m}{C_{gs} + C_{gd}}$$

$$f_T = \frac{g_m}{2\pi (C_{gs} + C_{gd})}$$

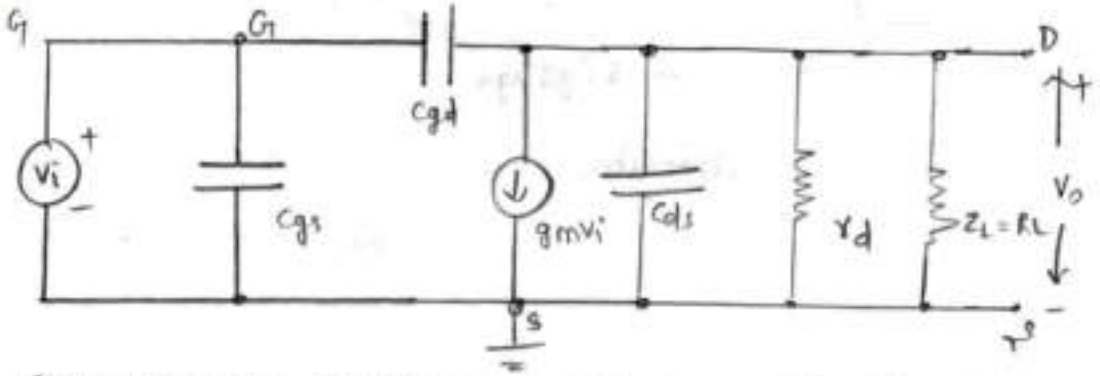
4.8.2. FREQUENCY RESPONSE OF COMMON SOURCE AMPLIFIER:



HIGH FREQUENCY CS AMPLIFIER

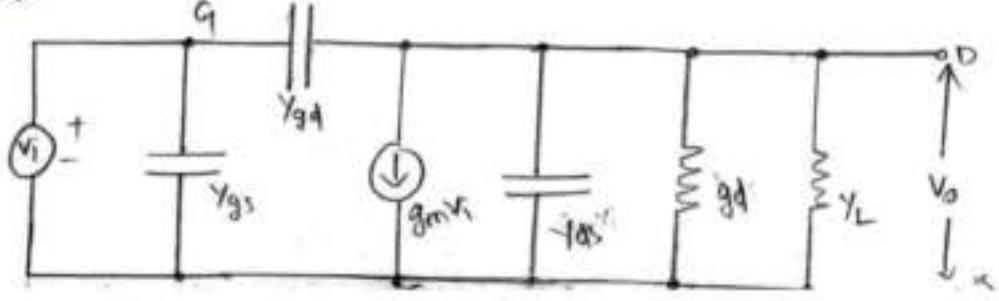
The circuit of configuration shows the cs amplifier

The equivalent circuit at high frequencies is shown in fig. below.

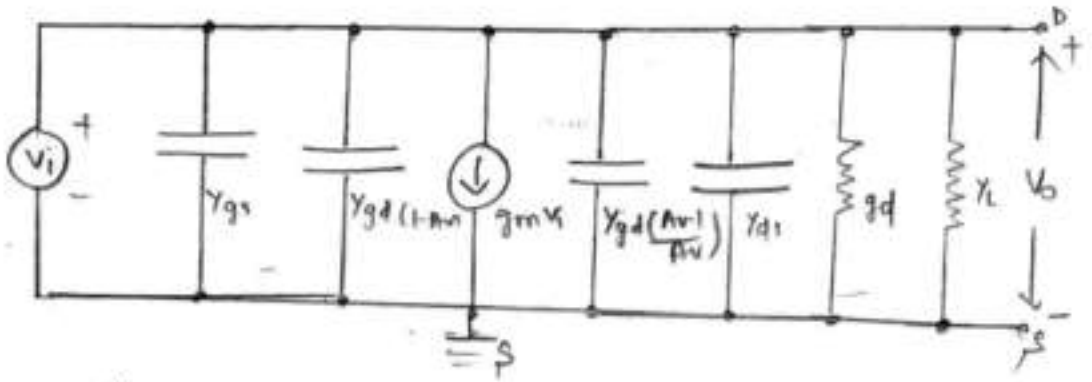


SHALL SIGNAL EQUIVALENT CIRCUIT OF CS AMPLIFIER AT HIGH FREQUENCIES

The equivalent circuit in terms of admittance is shown in Fig below.



Using Miller's Theorem, Y_{gd} connected between input and output has been separated to input & output sides respectively.



MILLER EQUIVALENT HIGH FREQUENCY ... CS AMPLIFIER

(i) INPUT ADMITTANCE, Y_i:

It is given by the parallel combination of Y_{gs} and $Y_{gd}(1-A_V)$.

$$Y_i = Y_{gs} + Y_{gd}(1-A_V)$$

(ii) OUTPUT ADMITTANCE, Y_o:

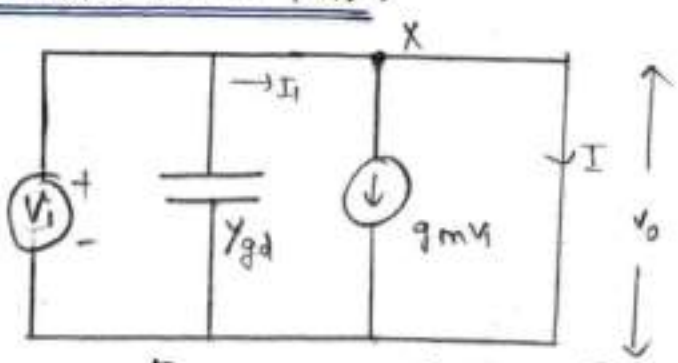
It is given by the parallel combination at the output side which includes $Y_{gd}\left(\frac{A_v-1}{A_v}\right)$, Y_{ds}, g_d and Y_L.

$$Y_o = Y_{gd}\left(\frac{A_v-1}{A_v}\right) + Y_{ds} + g_d + Y_L$$

Since $Y_{gd} << Y_{ds}$, Y_{gd} can be neglected

$$\therefore Y_o = Y_{ds} + g_d + Y_L$$

(iii) VOLTAGE GAIN, A_V:



EQUIVALENT CIRCUIT TO FIND A_V.

Apply Kirchoff's current law at node 'x'.

$$I_1 = g_m V_i + I \quad \rightarrow (1)$$

By ohm's law,

$$I = \frac{V}{R} = V_g$$

$$I_i = V_i Y_{gd} \quad \rightarrow (2)$$

$$\therefore V_i Y_{gd} = g_m V_i + I$$

$$I = V_i (Y_{gd} - g_m) \quad \rightarrow (3)$$

Voltage gain, $A_v = \frac{V_o}{V_i}$

$$= \frac{I Z}{V_i}$$

$$A_v = \frac{I}{Y V_i} \quad \rightarrow (4)$$

From output admittance

$$Y_o = Y_{gd} \left(1 - \frac{1}{A_v}\right) + Y_{ds} + g_d + Y_L$$

Since $\frac{1}{A_v} << 1$, it can be neglected

$$Y_o = Y_{gd} + Y_{ds} + g_d + Y_L \quad \rightarrow (5)$$

Substitute (3) & (5) in (4),

$$A_v = \frac{V_i (Y_{gd} - g_m)}{V_i (Y_{gd} + Y_{ds} + g_d + Y_L)}$$

$$A_v = \frac{Y_{gd} - g_m}{Y_{gd} + Y_{ds} + g_d + Y_L}$$

This is the equation of voltage gain at high frequency

At low frequency, capacitors are short circuited

$$\therefore A_V = \frac{-g_m}{g_d + Y_L}$$

$$= \frac{-g_m}{\frac{1}{r_d} + \frac{1}{Z_L}}$$

$$= \frac{-g_m r_d Z_L}{r_d + Z_L}$$

$$= -g_m (r_d \| Z_L)$$

Assume $Z_L' = R_D' = r_d \| Z_L$

$$\therefore A_V = -g_m Z_L' = -g_m R_D'$$

(iv) INPUT CAPACITANCE, C_i :

From Input admittance,

$$Y_i = Y_{gs} + Y_{gd}(1 - A_V)$$

We know that $A_V = -g_m R_D'$

$$\therefore Y_i = Y_{gs} + Y_{gd}(1 + g_m R_D') .$$

$\because C = 1/Y$, $Y = 1/C$,

From C_i,

$$\frac{1}{C_i} = \frac{1}{C_{gs}} + \frac{1}{C_{gd}(1 + g_m R_D')}$$

$$C_i = \frac{C_{gs} C_{gd}(1 + g_m R_D')}{C_{gs} + C_{gd}(1 + g_m R_D')}$$

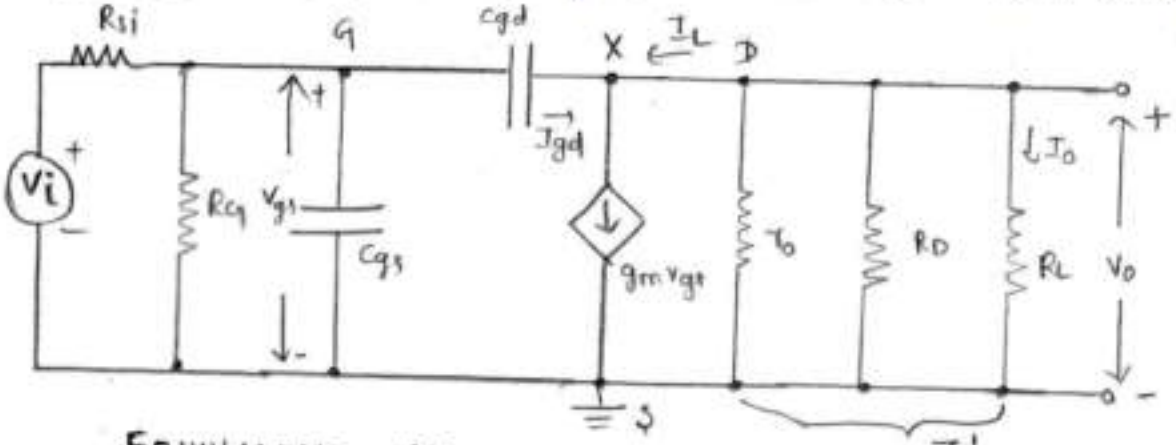
4.8.3. HIGH FREQUENCY RESPONSE :

Fig. shows the equivalent circuit for CS MOSFET Amplifie

Let us consider the output node. The load current is $g_m v_{gs} - I_{gd}$, where $g_m v_{gs}$ is the output current of MOSFET and I_{gd} is the current supplied through very small capacitance C_{gd}.

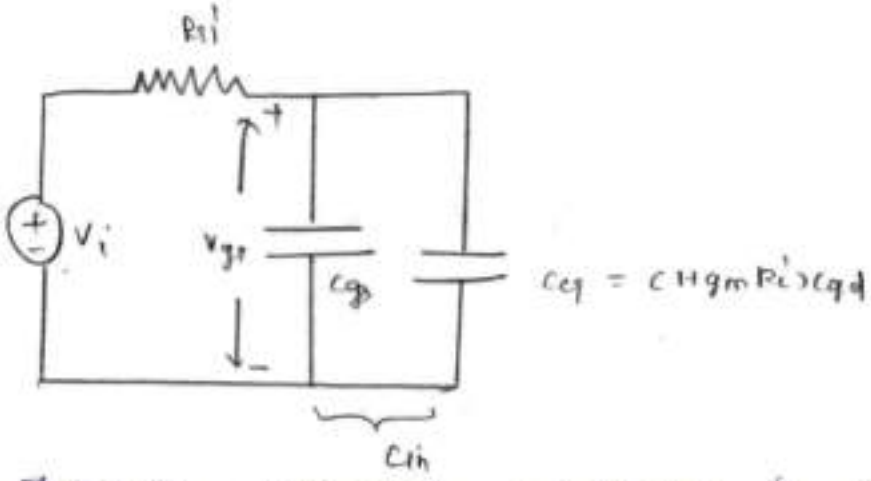
At frequencies in the vicinity of f_H, the I_{gd} is very small and can be neglected.

Hence, $V_o \cong -I_L R_L' = -g_m v_{gs} R_L'$ where $R_L' = r_o \| R_D \| R_L$



EQUIVALENT CIRCUIT OF CS MOSFET AMPLIFIER.

Now, consider the input node. We can replace C_{gd} at the input with the equivalent capacitance C_{eq} using Miller's Theorem.

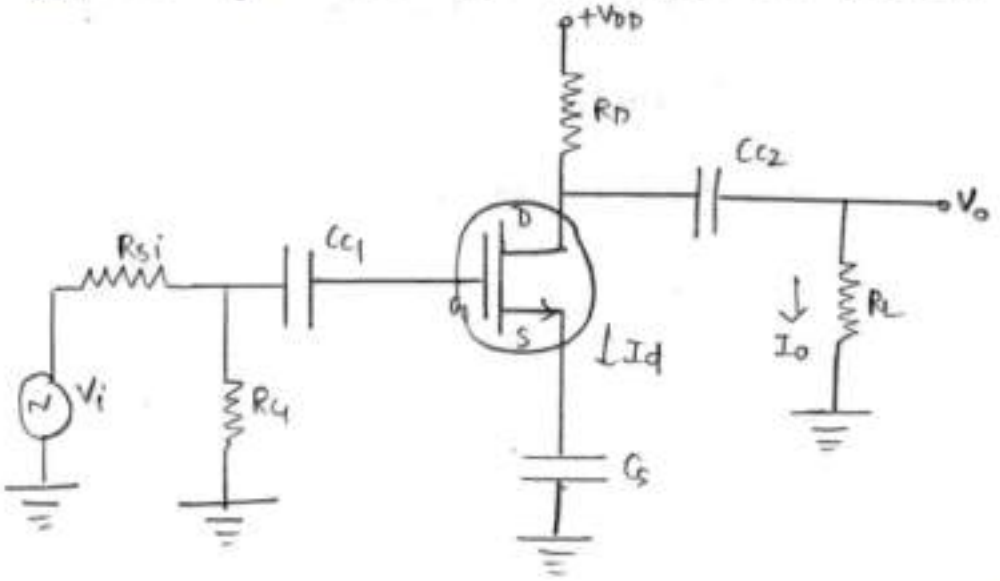


By Miller's Theorem, equivalent capacitance is given by

$$C_{eq} = [1+A_v)C = (1+A_v)C_{gd}$$

4.8.4. LOW FREQUENCY RESPONSE:

The low frequency response of CS MOSFET amplifier is affected by three RC networks as shown in the figure.



→ The first RC network is the input RC network due to input coupling capacitance, source resistance and gate resistance. The corner frequency due to input RC network is given by

$$f_1 = \frac{1}{2\pi C_{C_1}(R_{si} + R_G)}$$

→ The second RC network is the output RC network due to the output coupling capacitance, drain resistance and load resistance. The corner frequency due to output RC netwo is given by

$$f_1' = \frac{1}{2\pi(R_D + R_L) C_{C_2}}$$

→ The third RC network is due to the bypass capacitanc in the source terminal. The corner frequency due to the bypass RC network is given by

$$f_1'' = \frac{g_m}{2\pi C_S}$$

The highest among three frequencies is the lower 3 dB frequen

The parallel combination of r_o, R_D & R_L is given by Z_L'

$$Z_L' = r_o \| R_D \| R_L$$

Apply Kirchoff's current law at node 'X',

$$I_{gd} + I_L = g_m V_{gs}$$

Since $I_{gd} \ll I_L$, I_{gd} can be neglected

$$I_L = g_m V_{gs} \quad \rightarrow (1)$$

Voltage gain A_V is given by

$$A_V = \frac{V_o}{V_i} = \frac{V_o}{V_{gs}} \qquad [\because V_{gs} = V_i]$$

$$= \frac{I_o Z_L'}{V_{gs}}$$

$$= \frac{-I_L Z_L'}{V_{gs}}$$

$$= \frac{-g_m V_{gs} Z_L'}{V_{gs}}$$

$$\underline{A_V = -g_m Z_L'}$$

The total resistance at the input is given by

$$R_{si}' = R_{si} \| R_G$$

By considering input circuit as a simple time constant circuit

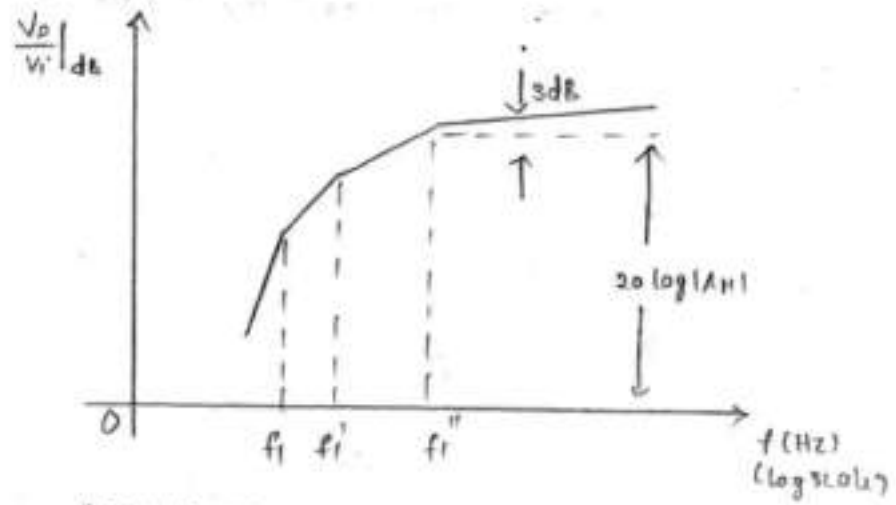
$$\tau = RC = R_{si}' C_{in}$$

where C_{in} is the total input capacitance given by

$$C_{in} = C_{gs} + C_{eq} = C_{gs} + C_{gd}(1 + g_m Z_L')$$

$$\omega_H = \omega_o = \frac{1}{\tau} = \frac{1}{R_{si}' C_{in}}$$

$$f_H = \frac{1}{2\pi R_{si}' C_{in}}$$



LOW FREQUENCY RESPONSE OF A CS MOSFET AMPLIFIER

Ex. Problem:

4.8.1. For a CS MOSFET Amplifier, $R_{si} = 120K\Omega$, $R_G = 4.7M\Omega$, $R_D = 10K\Omega$, $R_L = 15K\Omega$, $g_m = 1.2mA/V$, $r_o = 150K\Omega$, $C_{gs} = 1pF$ and $C_{gd} = 0.3pF$. Find the midband gain, Am and upper 3dB frequency, f_H.

Soln:

$$A_H = \frac{-R_G}{R_G + R_{si}} g_m R_L' \qquad [\because R_L' = Z_L']$$

where $R_L' = r_o \| R_D \| R_L$

$= 150 \| 10k \| 15k$

$= 5.77K\Omega$

$$A_H = -\frac{4.7 \times 10^6}{(4.7 \times 10^6) + (120 \times 10^3)} \times 1.2 \times 10^{-3} \times 5.77 \times 10^3$$

$A_H = -6.75$

$C_{eq} = C_{gd}(1 + g_m R_L')$

$= 0.3 \times 10^{-12} \times (1 + 1.2 \times 10^{-3} \times 5.77 \times 10^3)$

$C_{eq} = 2.377pF$

$\Rightarrow C_{in} = C_{eq} + C_{gs}$

$= (2.377 + 1)pF$

$C_{in} = 3.377pF$

$f_H = \frac{1}{2\pi R_{si}' C_{in}}$ where $R_{si}' = R_{si} \| R_G$

$= 120k \| 4.7M = 117K$

$= \frac{1}{\quad}$ .. $\Rightarrow$ f..

PROBLEM :-

Ex. 4.6.2. For a CS MOSFET amplifier, $C_{C_1} = C_S = C_{C_2} = 1\,\mu F$, $R_G = 12\,M\Omega$, $R_{si} = 180\,K\Omega$, $g_m = 1.2\,mA/V$, $R_D = 10\,K\Omega$ and $R_L = 15\,K\Omega$. Calculate A_M, f_1, f_1', f_1'' and f_L.

Soln: (i) $A_M = -\left(\frac{R_G}{R_{si} + R_G}\right) g_m R_L'$

$$R_L' = r_o \| R_D \| R_L$$

$$= R_D \| R_L$$

$$= 10K \| 15K$$

$$R_L' = 6K$$

$$= -\left[\frac{12}{12 + 0.18}\right] \times 1.2 \times 6 = -7.09$$

(ii) $f_1 = \frac{1}{2\pi (R_{si} + R_G) C_{C_1}}$

$$= \frac{1}{2\pi (180 \times 10^3 + 12 \times 10^6) \times 1 \times 10^{-6}}$$

$$f_1 = 0.013\,Hz$$

(iii) $f_1' = \frac{1}{2\pi (R_D + R_L) C_{C_2}}$

$$= \frac{1}{2\pi (25 \times 10^3) \times 1 \times 10^{-6}}$$

$$f_1' = 6.366\,Hz$$

(iv) $f_1'' = \frac{g_m}{2\pi C_S}$

$$= \frac{1.2 \times 10^{-3}}{2\pi \times 1 \times 10^{-6}}$$

$$f_1'' = 190.98\,Hz$$

Hence, f_1'' is larger among all other frequencies,

$$f_L = f_1'' = 190.98\,Hz$$

PROBLEM:-

Ex.4.8.3. Calculate the unity gain frequency with $g_m = 3mA/V$, $C_{gs} = 8pF$, $C_{gd} = 4pF$ and $C_{ds} = 1pF$.

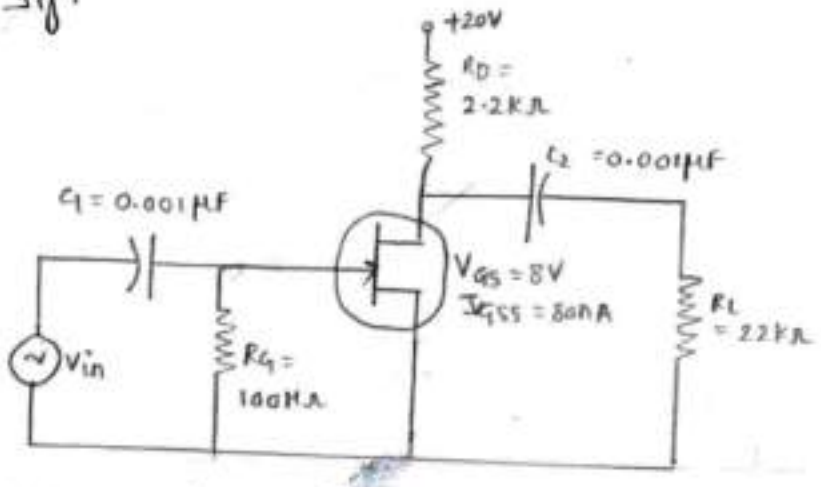
Soln: Unity gain frequency of MOSFET,

$$f_T = \frac{g_m}{2\pi (C_{gs} + C_{gd})}$$

$$= \frac{3 \times 10^{-3}}{2\pi (8+4) \times 10^{-12}}$$

$$f_T = 39.8 MHz$$

Ex.4.8.4. Determine the low frequency response of the amplifier circuit shown in fig.



Soln: It is necessary to analyse each network to determine the critical frequency of the amplifier.

(i) Input RC network:

$$f_c = \frac{1}{2\pi R_{in} C_1}$$

$$R_{in} = R_G \,||\, R_{in(gate)}$$

$$= R_G \,||\, \left[\frac{V_{GS}}{I_{GSS}}\right]$$

$$= 100M\Omega \,||\, \frac{8}{80 \times 10^{-9}}$$

$$= 100M \,||\, 100M$$

$$R_{in} = 50M\Omega$$

$$f_c = \frac{1}{2\pi \times 50 \times 10^6 \times 0.001 \times 10^{-6}} \Rightarrow f_c = 3.18 Hz$$

(ii) Output RC network:

$$f_c = \frac{1}{2\pi(R_D + R_L)C_2}$$

$$= \frac{1}{2\pi(2.2K + 22K) \times 1 \times 10^{-6}}$$

$$f_c = 6.577\ Hz$$

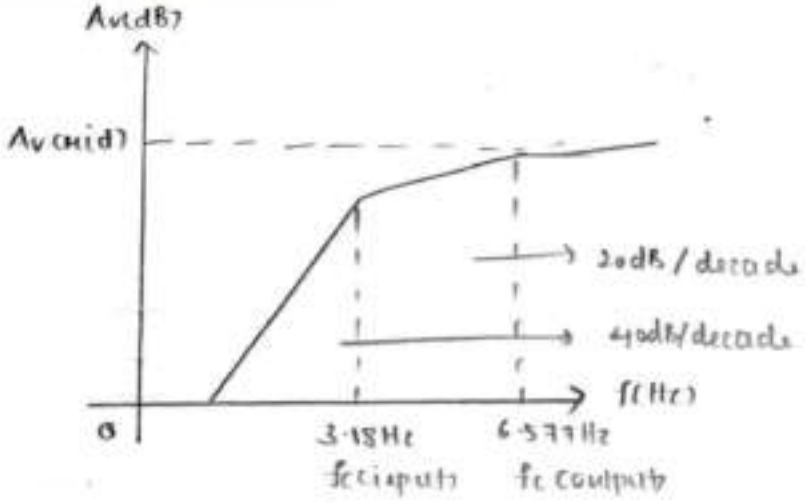
(iii) Bypass network:

Since there is no bypass RC network, it is not considered.

We have calculated two critical frequencies:

(i) f_c (input) = 3.18 Hz
(ii) f_c (output) = 6.577 Hz

It shows that the output network produces dominant lower critical frequency.



Ex.4.8.5. Calculate the unity gain bandwidth (or frequency with $g_m = 1.5mA/V$, $C_{gs} = 9pF$, $C_{gd} = 3pF$ and $C_{ds} = 1pF$

Sln. Unity gain frequency, $f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$

$$= \frac{1.5 \times 10^{-3}}{2\pi(9 + 3) \times 10^{-12}}$$

$$f_T = 19.89\ MHz$$

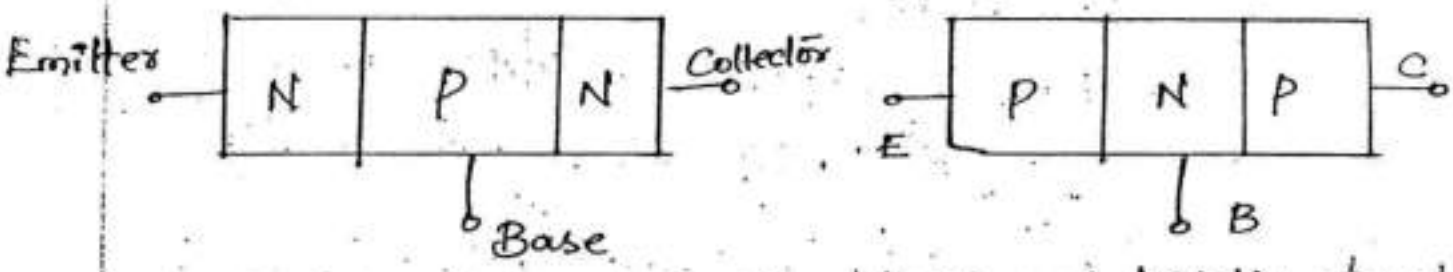
(*) BIPOLAR JUNCTION TRANSISTOR [BJT]

2m

Defn :- → Current conduction in Bipolar transistor because of both the types of charge carriers holes and electrons. Hence this is called Bipolar Junction transistor.

→ 2 Basic types are NPN, PNP.

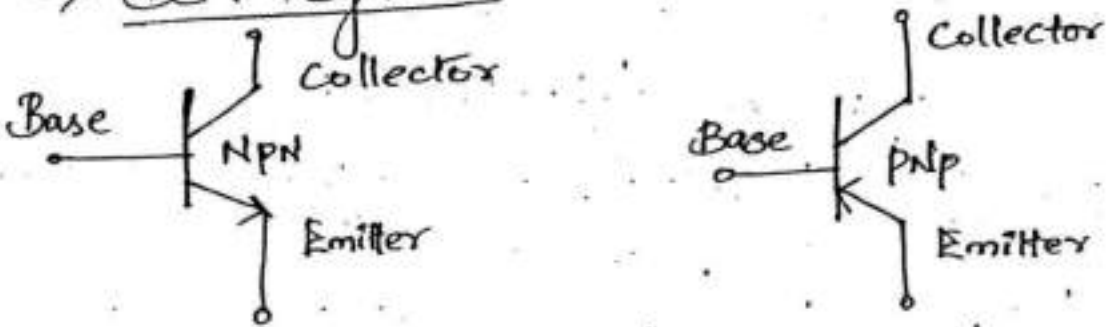
→ BJT construction :-



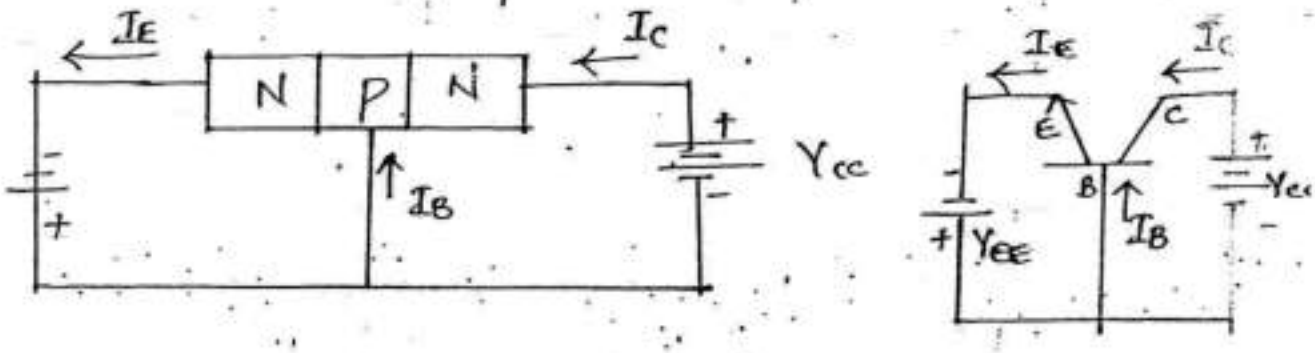
i) Base Region is very thin and lightly doped

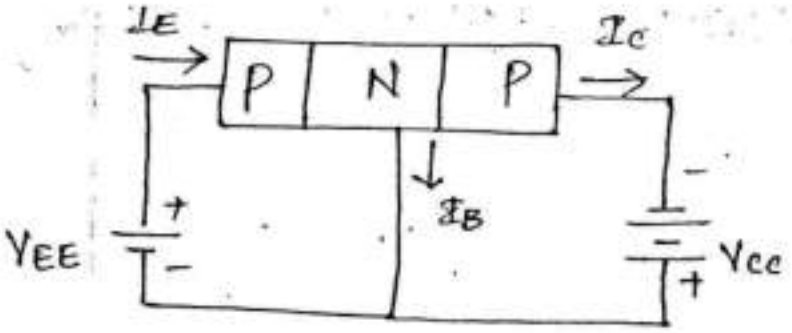
ii) Emitter and Collector region are heavily doped. But doping in emitter is greater than that of collector.

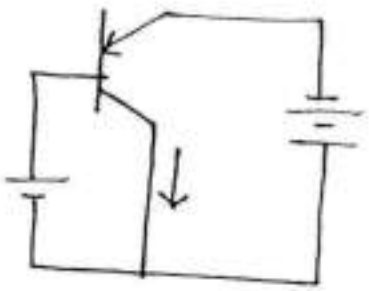
→ BJT Symbols :-



→ Transistor Conventional current directions







→ Electrons constitute the Emitter current "I_E"

→ Assume that 100 electrons are injected into the Base Region

→ Base Region is very thin (say two electrons) recombined with holes. This constitutes Base Current "I_B"

→ Remaining electrons, 98 appears in the collector. This constitutes Collector current "I_C".

→ Emitter Current I_E is always equal to the sum of Base and collector currents I_B and I_C.

) pblm ⟹ (*) $\boxed{I_E = I_B + I_C}$ ⟶ (1)

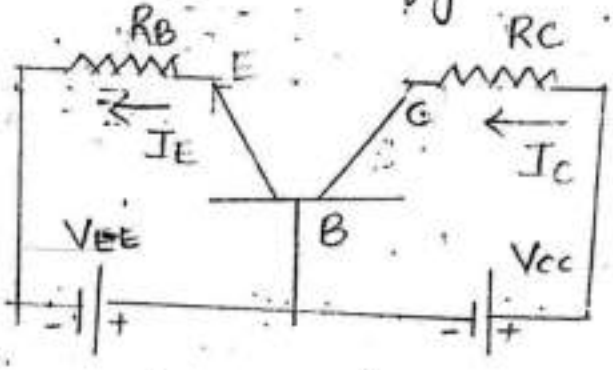
→ Since, I_B is very small. $I_E = I_C$.

→ **BJT Configurations:-**

1. Common Base
2. Common collector
3. Common Emitter

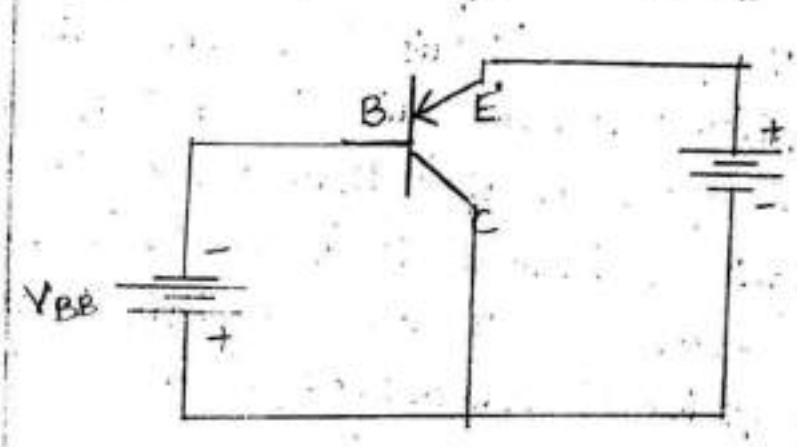
each (2m) drawing

1. Common Base Configuration :-



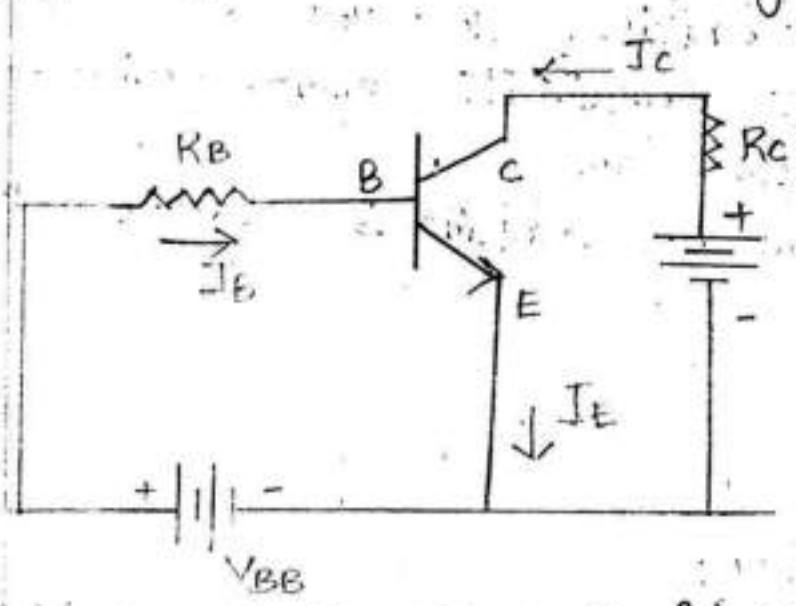
$\alpha = \frac{I_C}{I_B}$

2. Common collector Configuration :- (2m)



$$\gamma = \frac{I_E}{I_B}$$

3. Common Emitter Configuration :- (2m) (fig)



$$\beta = \frac{I_C}{I_B}$$

→ CE Mode, (2m)

Input Resistance	Low - R_B
output Resistance	High - R_C
Input current	I_B
output current	I_C
Input Voltage	V_{BE}
output Voltage	V_{CE}
Current Gain	High
Voltage Gain	High
Applications	Audio signal Amplification

Why CE Configuration is Widely used in Amplifier circuits ? (2m) (fig)

The CE Configuration is the only

Configuration which provides both Voltage gain as well as current gain greater than unity.
CB configuration Current gain less than unity
CC configuration Voltage gain is less than unity.
Power gain is much greater than other two Configura
Ratio of output Resistance to input Resistance is small, range from 10Ω to 100Ω. This Makes an ideal for coupling between transistor stages.

TOPIC I: DC LOAD LINE & OPERATING POINT :-

*) 8m What is DC Loadline? How you will Select the operating point, explain its Common Emitter Configu with an example. (8m)
M-04 i)
D-06
M-14

ii) Describe how D.C loadline is drawn? (8m)

Ans :-

- What is d.c biasing of the transistor? (2m)
- What is the Need for Biasing BJT?
- What is called operating point?

i) D.C Biasing :- (2m)

→ In Active Region, Emitter Base junction is forward biased and Collector Base junction is Reverse biased.

→ In order to operate transistor in the desired Region (Active Region), we have to apply external d.c voltage of correct polarity and Magnitude to the two junctions of the transistor.

→ Because d.c voltages are used to bias the transistor, biasing is known as d.c biasing of the transistor.

→ In transistor circuits, output signal

Power is always greater than input signal power.
→ The d.c sources (d.c biasing) supplies the power to the transistor circuit to get the output signal power greater than input signal power.

ii) → When we Bias a transistor we establish a certain current and voltage conditions for the transistor. These conditions are known as operating conditions (or) d.c operating point (or) Quiescent point.

(2m) (X)

→ The operating point must be stable for proper operation of the transistor.
→ operating point shifts with changes in transistor parameters such as β, [current gain],
Ico [Reverse Saturation current]
V_{BE} [Base Emitter Voltage]

(X) (2m)

→ As transistor parameters are temperature dependent, operating point also varies with changes in temperature.

(2m) Defn:

→ for proper operation of transistor, fixed level of current and voltage in the transistor defined a point at which transistor operates. This point is called operating point (or) Quiescent (or) Q-point in Active region.

(*) Draw and explain "fixed Bias" circuit.

D-09 (6m)

Ans:- → Let us consider fixed Bias circuit, For d.c. Analysis, Replace capacitor with an open circuit because Reactance of a capacitor for d.c

$X_C = 1/2\pi fc \Rightarrow 1/2\pi(0) = \infty$.

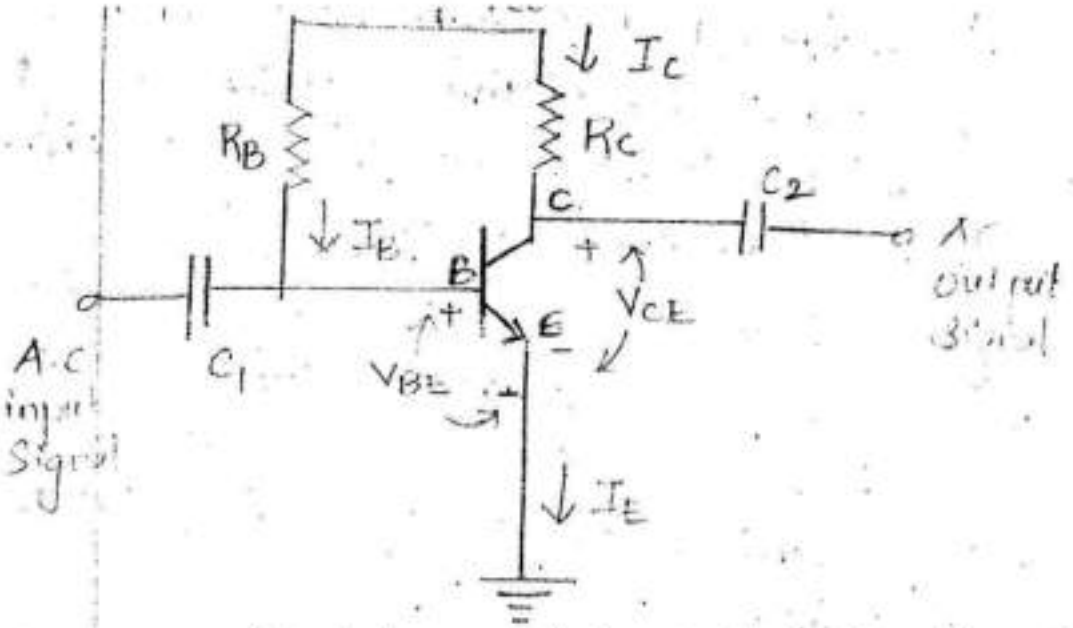
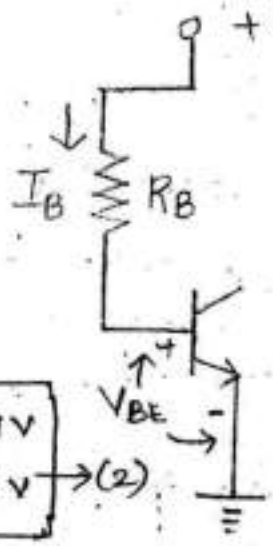


fig (a) fixed Bias circuit

CIRCUIT ANALYSIS :-

i) Base circuit of the fixed Bias circuit :-



Applying Kirchoff's Voltage law to the Base circuit,

$V_{cc} - I_B R_B - V_{BE} = 0$

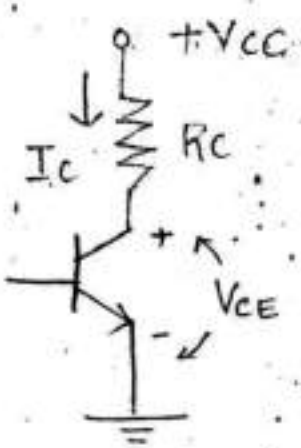
$V_{cc} - V_{BE} = I_B R_B$

$$I_B = \frac{V_{cc} - V_{BE}}{R_B} \rightarrow (1)$$

Si → $V_{BE} = 0.7V$

Ge → $V_{BE} = 0.3V$ → (2)

ii) collector circuit of the fixed Bias circuit :-



Applying Kirchoff's Voltage law to the collector circuit,

$V_{cc} - I_C R_C - V_{CE} = 0$

$$V_{CE} = V_{cc} - I_C R_C \rightarrow (3)$$

$V_{cc} - V_{CE} = I_C R_C$

$$I_C = \frac{V_{cc} - V_{CE}}{R_C} \rightarrow (4)$$

(iii) current gain factor, $\beta = \frac{I_C}{I_B}$ ⟶ (5)

iv) $V_{BE} = V_B - V_E$ ⟶ (a)

$V_{CE} = V_C - V_E$ ⟶ (b)

$V_B \rightarrow$ Base Voltage

$V_E \rightarrow$ Emitter Voltage

$V_C \rightarrow$ Collector Voltage

$\therefore V_E = 0$ (in the circuit)

$\therefore V_{BE} = V_B$ (from a)

$V_{CE} = V_C$ (from b)

→ Base current I_B is controlled by R_B.

→ collector current I_C is not a function of R_C.

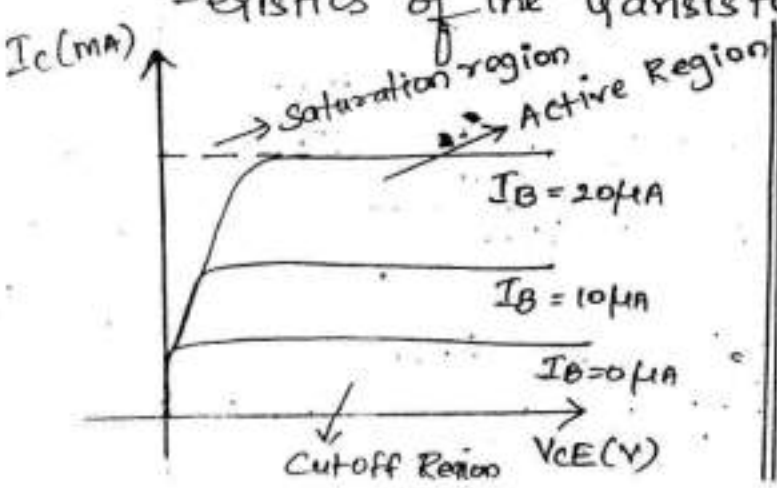
→ change R_C to any level will not affect I_B(or) I_C in Active region.

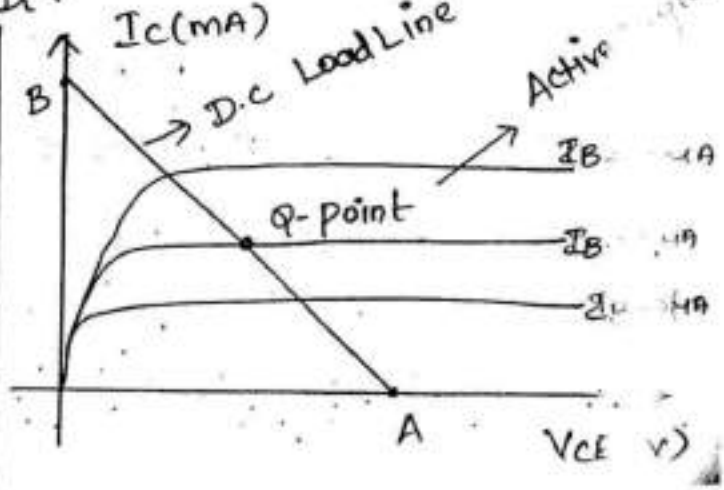
Proper Biasing :-

Transistor is used as an amplifier, the Q point should be selected at the centre of the DC loadline to prevent any possible distortion.

(X) What is meant by Loadline ? (2m)

Ans: A D.C Loadline of a transistor is the straight line drawn on the output characteristics of the transistor.





for fixed Bias Circuits,

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

$$= \frac{V_{CC}}{R_C} - \left(\frac{1}{R_C}\right) V_{CE}$$

$$I_C = -\left(\frac{1}{R_C}\right) V_{CE} + \frac{V_{CC}}{R_C} \longrightarrow (A)$$

Equation of Straight line, $y = mx + c \longrightarrow (B)$

To determine the two points ('A' and 'B'), we assume

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} \longrightarrow (C)$$

at 'A', a) $V_{CE} = V_{CC}$ in (C), $I_C = \frac{V_{CC} - V_{CC}}{R_C}$, $I_C = 0$

at 'B', b) $V_{CE} = 0$, in (C), $I_C = \frac{V_{CC} - 0}{R_C}$, $I_C = \frac{V_{CC}}{R_C}$

$I_C = \frac{V_{CC}}{R_C}$

1:- Load Line

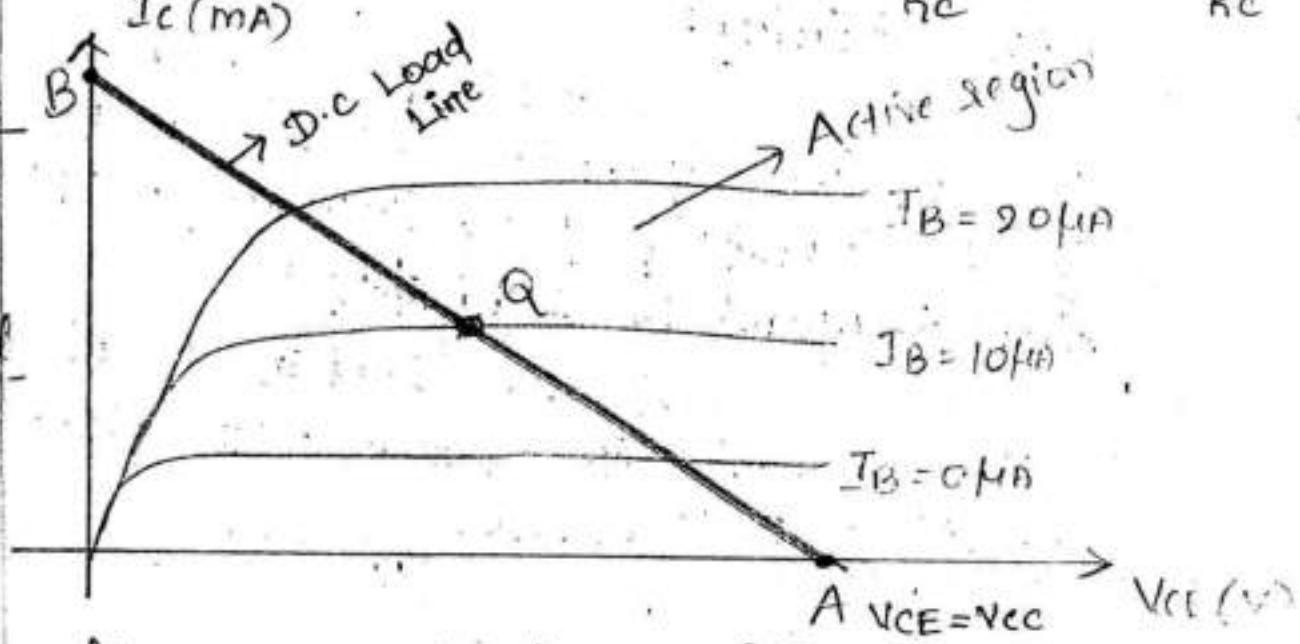


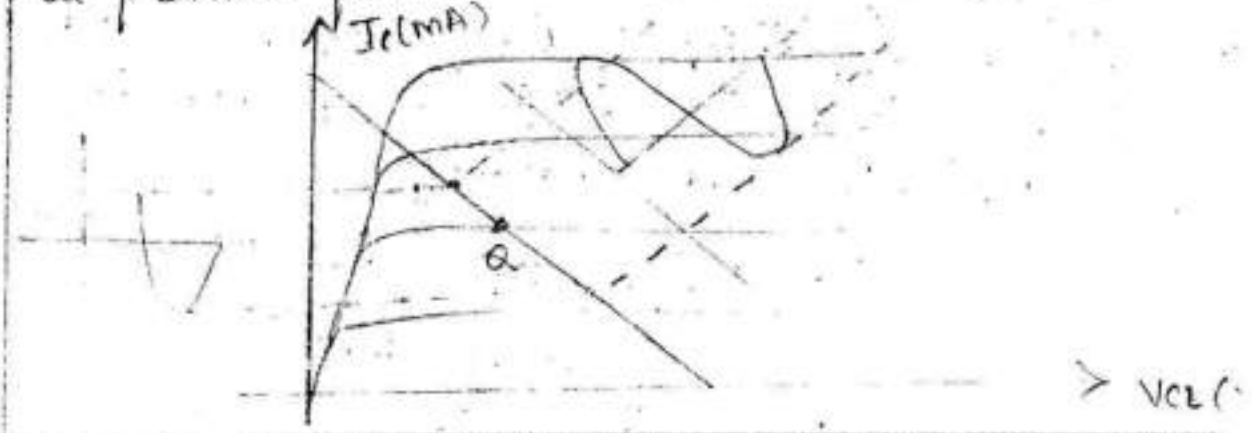
fig:- CE-output characteristics with d.c load line

→ Line drawn between points 'A' and 'B' is called d.c. Loadline.

→ 'd.c' indicates (i.e) input signal is assumed to be zero.

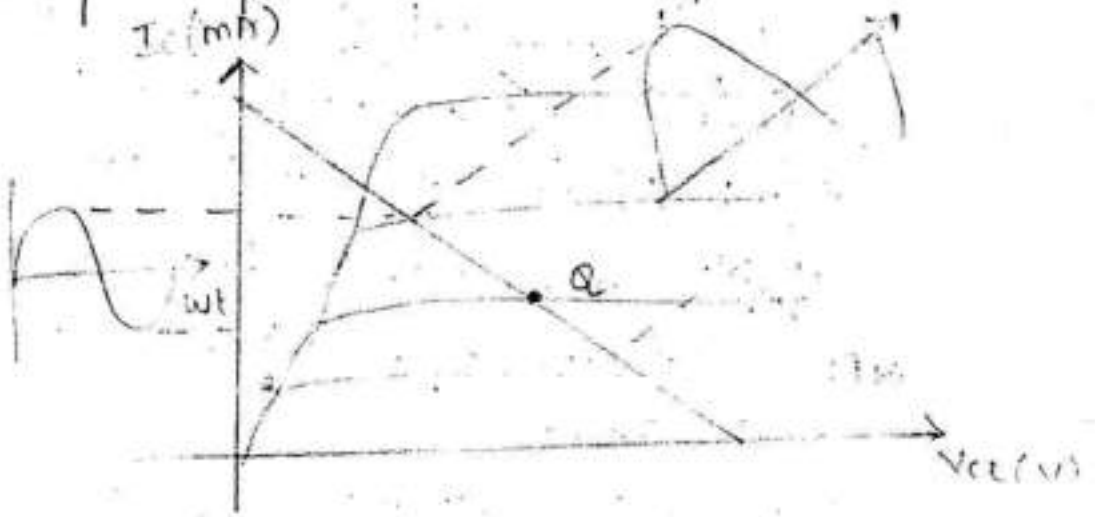
(*) SELECTION OF OPERATING POINT :-

ase(i) Operating point near Saturation region gives clipp... at positive peaks.



ase(ii) operating point near cut-off region gives clipping at Negative peaks.

use(iii) operating point at the centre of Active re... is most suitable.



VBE for Si = 0.7V, Ge = 0.3V.

VARIATION OF QUIESCENT POINT:-

Defn: (2m)

→ Designing the Biasing circuit, care should be taken so that the operating point will not shift into an undesirable region [cut-off & Saturation region]. Hence biasing the circuit to stabilize the Q-point is known as Bias stability.

→ 2 important factors are
- i) Temperature
- ii) h_{fe}/β.

i) Temperature :-

a) I_{CO} :- flow of current in the circuit produces heat at the junctions. This heat increases the temperature at the junctions.

$$I_C = \beta I_B + I_{CEO}$$

Power dissipation, $P_D = V_C I_C$

→ Heat (Excess) produced at the collector base junction may even burn and destroy the transistor. This situation is called "Thermal Runaway".

→ for any transistor, Maximum power dissipation is always a fixed value. This is known as 'Maximum power Dissipation' rating of a transistor.

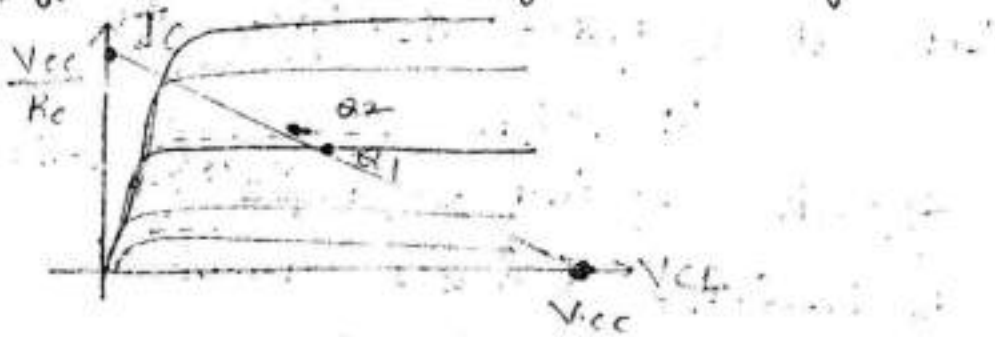
b) V_{BE} :- V_{BE} changes with temperature at the rate of 2.5mV/°C. I_B depends on V_{BE}. I_C depends on I_B, V_{BE}.

c) β :- It is temperature dependent. β varies I_C varies, $I_C = \beta I_B$. Change in I_C change the operating point.

→ Avoid the thermal instability, biasing the circuit should be designed to provide a degree of temperature stability.

ii) Transistor current gain h_{FE}/β :-

→ Changes in the transistor parameters among different units of the same type, same number.



(*) Advantages of fixed Bias :-

→ Simple circuit because of few components
→ operating point can be fixed anywhere in the Active Region
→ Maximum flexibility in the design.

(*) AC LOAD LINE :-

Q.VII :- Explain Ac Load Line with diagram ? Draw it

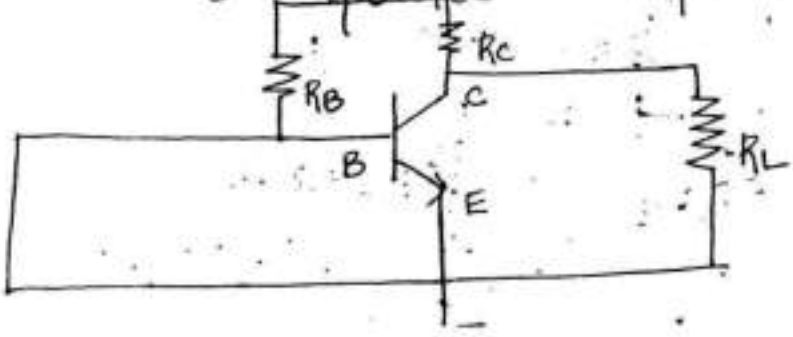
M-12 (4m)

Ans :- → position of Q-point is constant when we do Ac Analysis (or) DC Analysis.

→ capacitor act as short circuit.

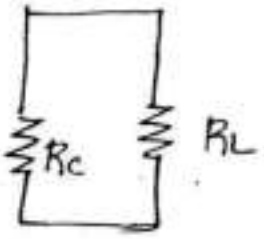
$$X_C = \frac{1}{2\pi fC} \quad f \uparrow \; X_C \downarrow.$$

→ DC source → shorted.



R_C and R_L are parallel. Hence it act as a effective resistance.

$$R_{ac} = R_C \parallel R_L$$



$$\text{Slope} = -\frac{1}{R_{ac}}$$

$R_C > R_{ac}$

Eg:- If $R_C = 1K\Omega$, $R_L = 1K\Omega$, $R_{ac} = 0.5K\Omega$

$R_C > R_{ac}$

Effective Resistance decreases, Voltage decreas [V = IR]

If Resistance decreases current increases [V = IR]

$$\text{Max. } V_{CE}' = V_{CEQ} + I_{CQ} \cdot R_{ac}$$

$$\text{Max } I_C = I_{CQ} + \frac{V_{CQE}}{R_{ac}}$$

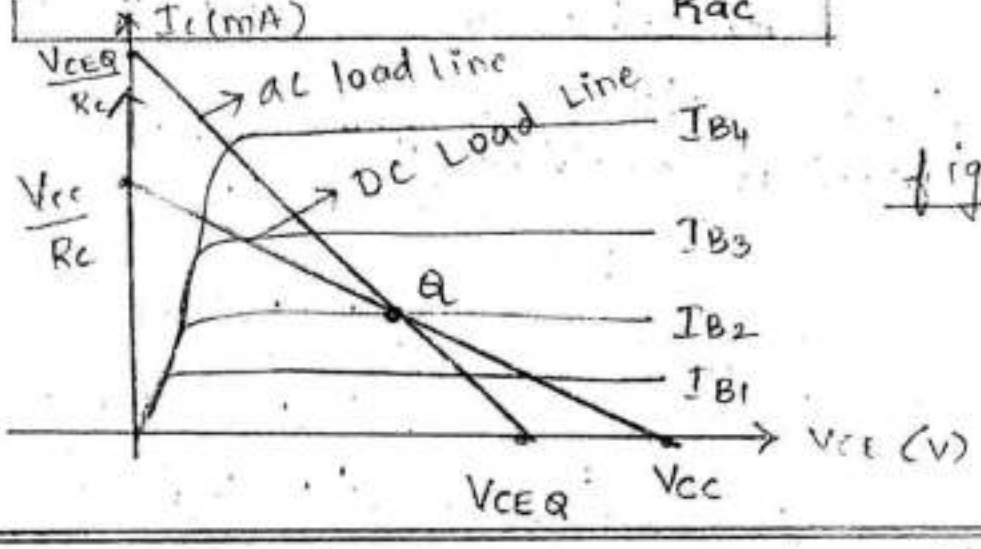
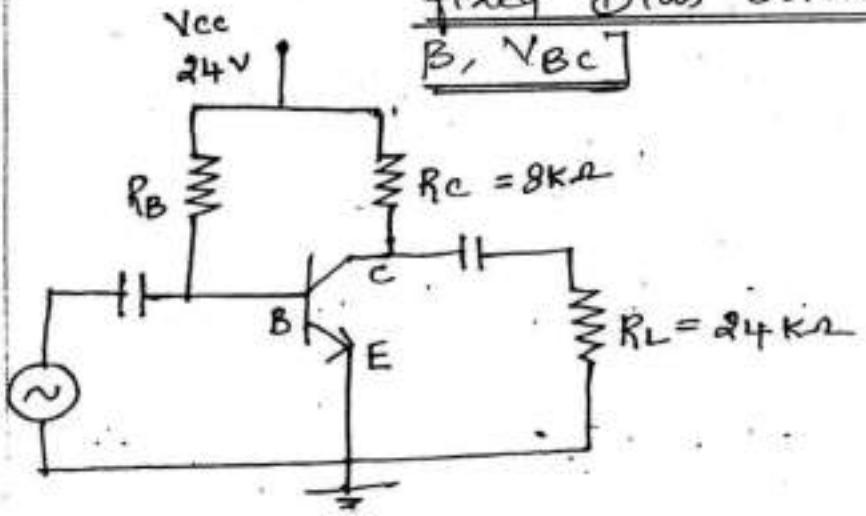


fig:- AC / ...

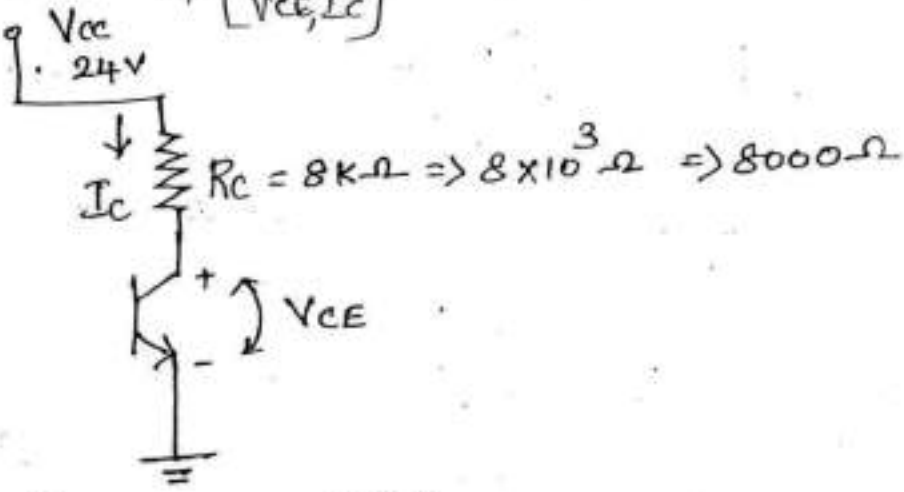
PROBLEMS [AC / DC Load Line / operating 'Q' point / fixed Bias circuit / IB, IC, VCE, VBE / β, VBC]

① 

From the above circuit, $R_C = 8K\Omega$, $R_L = 24K\Omega$ and $V_{CC} = 24V$. Draw the DC Load Line and Determine the operating point Values. Also Find the AC Load Line. [V_{CE}, I_C]

Soln: A) DC Load Line

Apply KVL to the collector circuit,



$$V_{CC} - I_C R_C - V_{CE} = 0 \longrightarrow (1)$$

i) Find V_{CE} :- [$I_C \to 0$]

from eqn(1) $\Rightarrow$ $24 - I_C \times 8000 - V_{CE} = 0$

$$24 - (0) - V_{CE} = 0$$

$$\boxed{V_{CE} = 24V}$$

ii) Find I_C :- [$V_{CE} \to 0$]

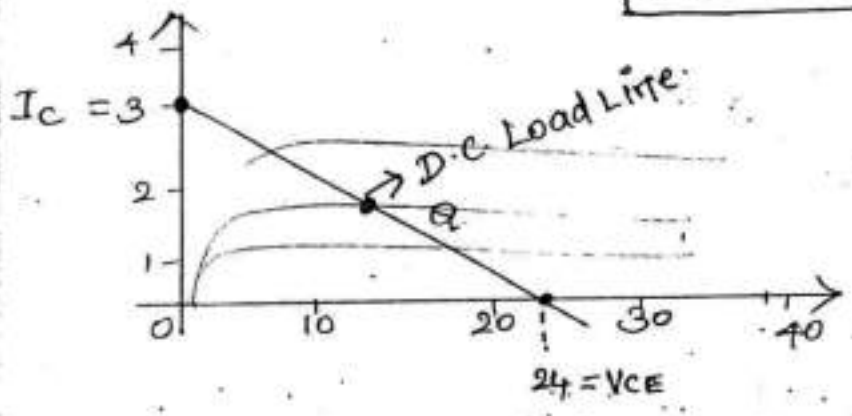
from eqn(1) $\Rightarrow$ $24 - I_C \times 8000 - V_{CE} = 0$

$$24 - I_C \times 8000 - 0$$

$$I_C = \frac{24}{8000}$$

$$\boxed{I_C = 3 \times 10^{-3} A}$$

$$\boxed{I_C = 3mA}$$



B) For AC Load Line :-

i) Max $V_{CE} = V_{CEQ} + I_{CQ} \cdot R_{ac}$

Max $V_{CE} = 12 + 1.5\, R_{ac}$ ⟶ (A)

ii) $V_{CEQ} = \frac{V_{CE}}{2} = \frac{24}{2} = 12V$

iii) $I_{CQ} = \frac{I_C}{2} = \frac{3mA}{2} = 1.5mA$

iv) $R_{ac} = R_C \parallel R_L$ ⟶

$R_C = 8K\Omega$, $R_L = 24K\Omega$

$= 8K \parallel 24K$

$\boxed{R_C = 6K\Omega}$

Resistor in ||el

$\frac{1}{R_p} = \frac{1}{R_1} + \frac{1}{R_2}$

$\frac{1}{R_p} = \frac{R_2 + R_1}{R_1 R_2}$

$R_p = \frac{R_1 R_2}{R_1 + R_2}$

$R_p = \frac{8 \times 24}{8+24}$

$R_c = \frac{192}{32}$

$\boxed{R_c = 6K\Omega}$

Sub in (A).

Max $V_{CE} = 12 + 1.5 \times 6 \times 10^3$

$\boxed{\text{Max } V_{CE} = 21V}$

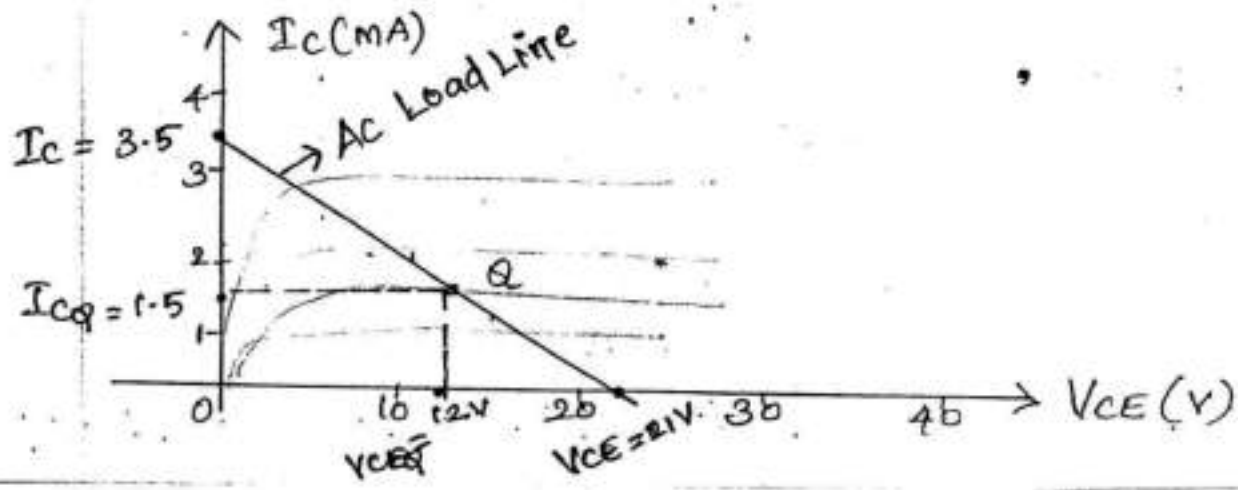
Max $I_C = I_{CQ} + \frac{V_{CEQ}}{R_{ac}}$

$= 1.5 \times 10^{-3} + \frac{12}{6 \times 10^3}$

$= 1.5 \times 10^{-3} + 2 \times 10^{-3}$

$\boxed{\text{Max } I_C = 3.5 \times 10^{-3} A}$

$\boxed{\text{Max } I_C = 3.5mA}$



(2) Draw the D.C Load Line, find I_C and V_{CE}. Given $R_C = 12K\Omega$, $V_{CC} = 20V$ for fixed bias.

Soln:- From the Fixed Bias circuit,

$$V_{CC} - I_C R_C - V_{CE} = 0 \longrightarrow (1)$$

Find V_{CE}:- i) put $I_C = 0$ in (1) [pt 'A']

$$V_{CC} - 0 - V_{CE} = 0.$$

$$V_{CC} = V_{CE}$$

$$\boxed{V_{CE} = 20V}$$

ii) Find I_C :- put $V_{CE} = 0$ in (1) [pt 'B']

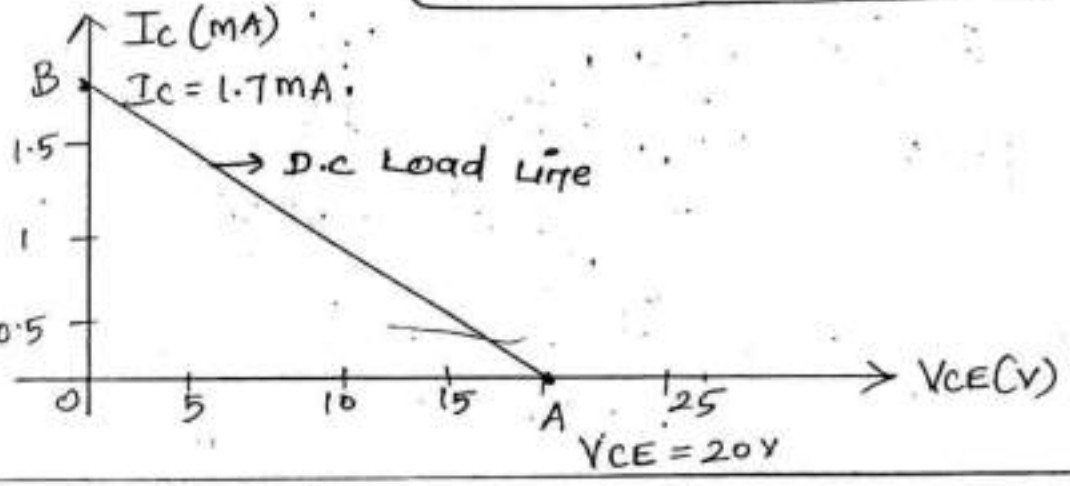
$$V_{CC} - I_C R_C - 0 = 0$$

$$V_{CC} = I_C R_C$$

$$I_C = \frac{V_{CC}}{R_C}$$

$$I_C = \frac{20}{12 \times 10^3}$$

$$\boxed{I_C = 1.7 \times 10^{-3} A \text{ (or) } 1.7mA.}$$



(3) Find the points 'A' and 'B' for the given fixed b Values, $V_{CC} = 20V$, $R_C = 10K\Omega$.

Soln:- i) Find V_{CE}:- (pt 'A') $I_C = 0$:

$$V_{CC} - V_{CE} - I_C R_C = 0$$

$$V_{CC} - V_{CE} - 0 = 0$$

$$\therefore V_{CC} = V_{CE} \Rightarrow \boxed{V_{CE} = 20V}$$

ii) Find I_C :- [put $V_{CE} = 0$] pt 'B'

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$-V_{CC} - I_C R_C = 0$$

$$I_C = \frac{V_{CC}}{R_C} = \frac{20}{10 \times 10^3}$$

$$\therefore \boxed{I_C = 2 \times 10^{-3} A \text{ (or) } 2mA}$$

④ Draw the Load Line for the fixed bias ckt $I_B = 20\mu A$, $V_{CC} = 20V$, $R_C = 10K\Omega$, $\beta =$

Soln:-

i) $\beta = \frac{I_C}{I_B}$

Find I_C :-

pt 'B'

$$\beta \times I_B = I_C$$

$$I_C = 50 \times 20 \times 10^{-6}$$

$$I_C = 1000 \times 10^{-6}$$

$$\boxed{I_C = 1 \times 10^{-3} \text{ (or) } 1mA}$$

ii) Find V_{CE} :-

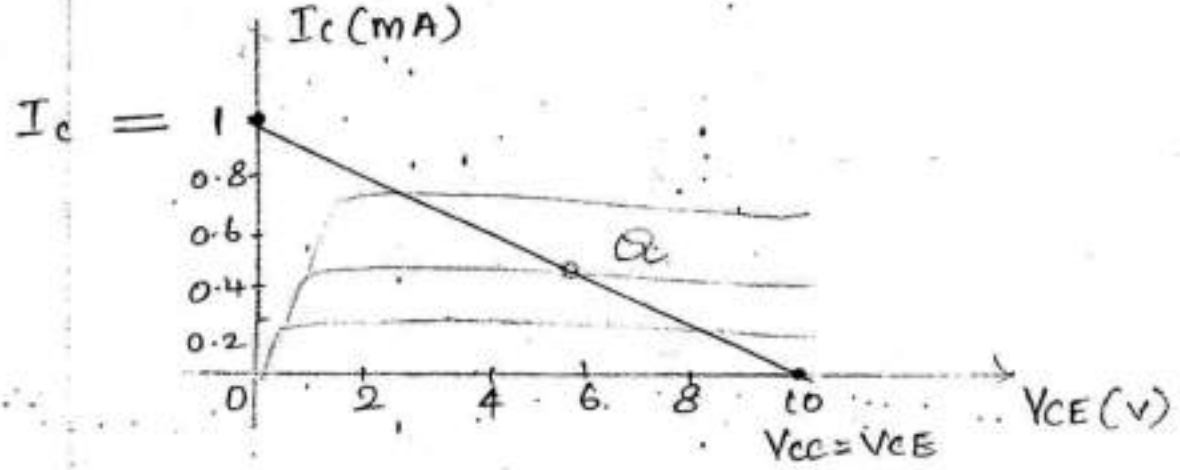
pt 'A'

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$20 - (1 \times 10^{-3}) \times (10 \times 10^3) = V_{CE}$$

$$20 - 10 = V_{CE}$$

$$\boxed{V_{CE} = 10V}$$



(5) $I_B = 30\mu A$, $\beta = 50$, $V_{CC} = 20V$, $R_C = 10K\Omega$. find V_{CE} and I_C ?

Soln:- i) Find V_{CE} :- [Put Point 'A']

$$V_{CC} - V_{CE} - I_C R_C = 0 \quad \text{——} (1)$$

ii) $\beta = \frac{I_C}{I_B}$

$$I_C = \beta \cdot I_B$$

$$= 50 \times 30 \times 10^{-6}$$

$$\boxed{I_C = 1.5 \times 10^{-3} \text{ (or) } 1.5mA} \longrightarrow (2)$$

Sub (2) in (1)

$$20 - V_{CE} - (1.5 \times 10^{-3}) \times (10 \times 10^{3})$$

$$V_{CE} = 20 - 15$$

$$\boxed{V_{CE} = 5V}$$

---

(6) Design a Fixed Bias circuit using a Silicon transistor having β value of 100. V_{CC} is 10V. and d.c bias conditions are to be $V_{CE} = 5V$ and $I_C = 5$

Soln:- Given :- $\beta = 100$

$V_{CC} = 10V$

$V_{CE} = 5V$

$I_C = 5mA$

i) Apply KVL in collector circuit,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

find R.C, $R_C = \frac{V_{CC} - V_{CE}}{I_C}$

$$= \frac{10 - 5}{5 \times 10^{-3}} \Rightarrow \frac{5}{5 \times 10^{-3}}$$

$$\boxed{R_C = 1K\Omega}$$

ii) $\beta = \frac{I_C}{I_B}$

$$I_B = \frac{I_C}{\beta} = \frac{5 \times 10^{-3}}{100}$$

$$\boxed{I_B = 50 \times 10^{-6} \text{ (or) } 50\mu A}$$

(iii) Applying KVL in the Base circuit,

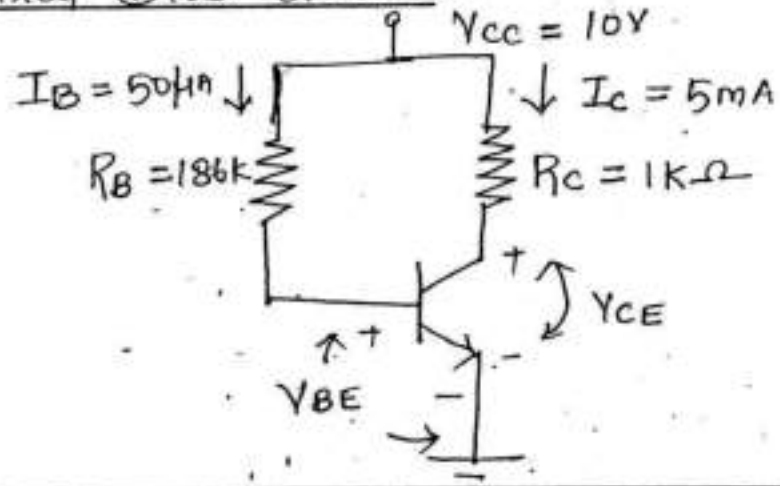
$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} \qquad [V_{BE} = 0.7\,V \text{ for Si}]$$

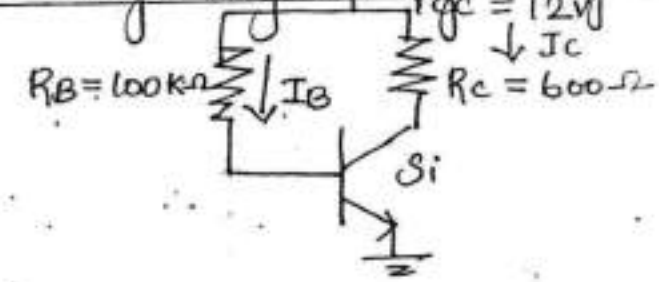
$$= \frac{10 - 0.7}{50 \times 10^{-6}}$$

$$\boxed{R_B = 186 \times 10^3 \text{ (or) } 186K\Omega}$$

Fixed Bias circuit :-



(7) The Fixed Biased circuit in Fig is subjected to an increase in junction temperature from 25°C to 75°C. If $\beta = 100$ at 25°C and $\beta = 125$ at 75°C, determine Percent change in Q point values (V_{CE}, I_C) over the temperature range. Neglect any change in V_{BE}.



Sol(i):- At 25°C,

i) Apply KVL to Base ckt,

$V_{CC} - I_B R_B - V_{BE} = 0$

$I_B = \frac{V_{CC} - V_{BE}}{R_B}$

$I_B = \frac{12 - 0.7}{100 \times 10^3}$

$I_B = 113 \times 10^{-6}$ (or) $I_B = 113\ \mu A$

ii) Apply KVL to collector ckt,

$V_{CC} - I_C R_C - V_{CE} = 0$

$V_{CE} = V_{CC} - I_C R_C$

$V_{CE} = 12 - (11.3 \times 10^{-3}) \times 600$

$V_{CE} = 5.22\ V$

$\beta = \frac{I_C}{I_B}$, $I_C = \beta I_B$

$I_C = 100 \times 113 \times 10^{-6}$

$I_C = 11.3 \times 10^{-3}$ (or) $I_C = 113\ mA$

At 75°C,

i) $I_B = 113\ \mu A$

$I_C = \beta \cdot I_B$

$= 125 \times 113 \times 10^{-6}$

$I_C = 14.125 \times 10^{-3}$ (or) $I_C = 14.125\ mA$

ii) Apply KVL to collector ckt,

$V_{CC} - I_C R_C - V_{CE} = 0$

$V_{CE} = V_{CC} - I_C R_C$

$V_{CE} = 12 - (14.125 \times 10^{-3}) \times 600$

$V_{CE} = 3.525\ V$

$$\% \text{ change in } I_C = \frac{I_C(75^\circ C) - I_C(25^\circ C)}{I_C(25^\circ C)} \times 100\%$$

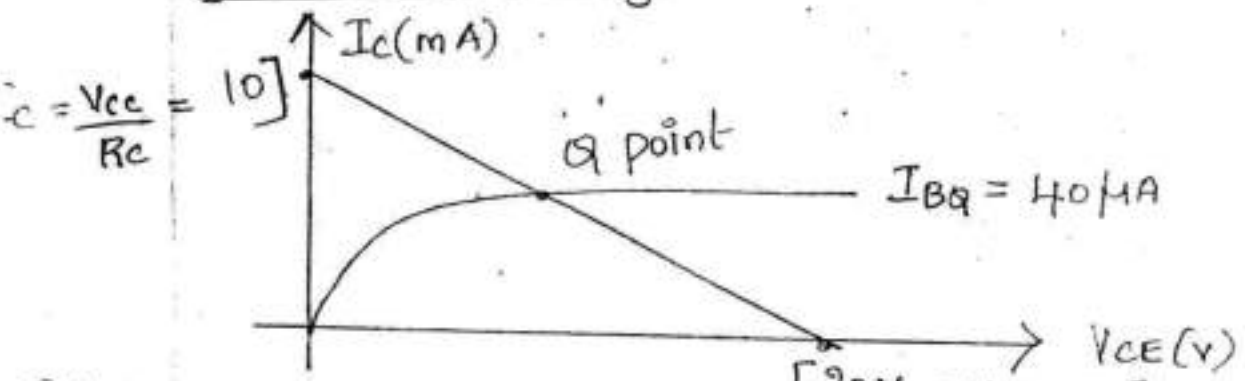
$$= \frac{(14.125 \times 10^{-3}) - (11.3 \times 10^{-3})}{(11.3 \times 10^{-3})} \times 100\%$$

$$\% \text{ change in } V_{CE} = 25\% \text{ (an increase)}$$

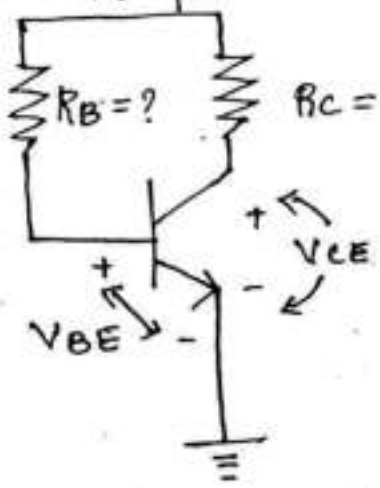
$$= \frac{V_{CE}(75^\circ C) - V_{CE}(25^\circ C)}{V_{CE}(25^\circ C)} \times 100\%$$

$$= \frac{3.525 - 5.22}{} \times 100\% \Rightarrow -32.47\% \text{ (a decrease)}$$

(8) Design the fixed bias circuit from the ... given in the fig. (16)



Solⁿ :- i) Fixed Bias Ckt,



ii) Find Rc :-

$V_{CE} = V_{cc} = 20V$

$I_C = \frac{V_{cc}}{R_c} = 10 \times 10^{-3}$

$10 \times 10^{-3} = \frac{20}{R_C}$

$R_c = \frac{20}{10 \times 10^{-3}}$

$\boxed{R_c = 2k\Omega}$

iii) Apply KVL at Base Ckt,

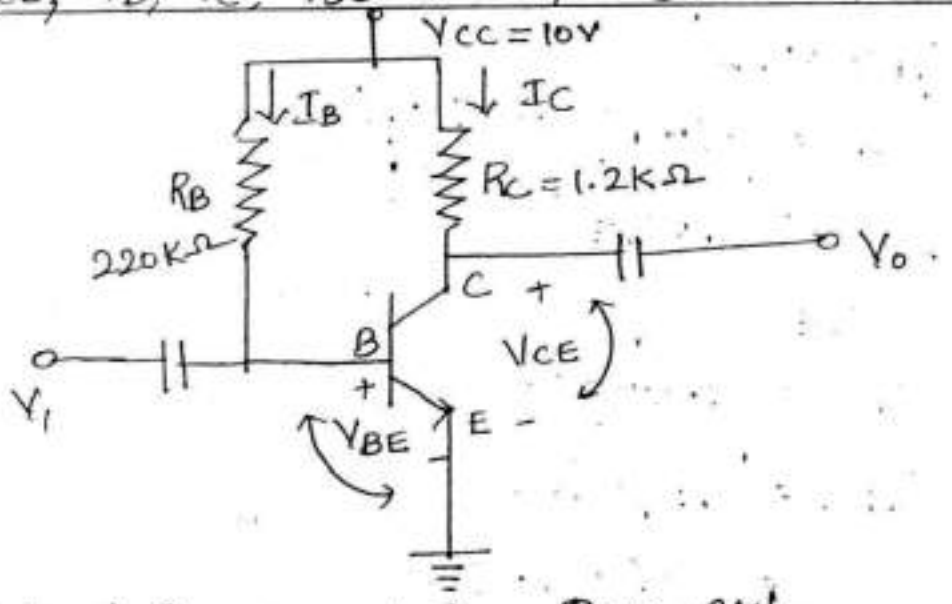
[$\because V_{BE} = 0.7$, $I_B = 40\mu A$ from fig.]

$V_{cc} - I_B R_B - V_{BE} = 0$

$R_B = \frac{V_{cc} - V_{BE}}{I_B} \Rightarrow \frac{20 - 0.7}{40 \times 10^{-6}}$

$\boxed{R_B = 482.5\ k\Omega}$

(9) For the circuit shown in the fig, calculate I_B, V_{CE}, V_B, V_C, V_{BC}. Assume $V_{BE} = 0.7V$ and $\beta = 50$



Soln :- i) Applying KVL to the Base ckt,

I_B :-

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_B = \frac{10 - 0.7}{220 \times 10^3} = \frac{0.3 \times 10^{-3}}{220}$$

$$I_B = 42.27 \times 10^{-6} \text{ (or) } 42.27 \mu A$$

ii) $\beta = \frac{I_C}{I_B}$

I_C :-

$$I_B = \frac{I_C}{\beta} \Rightarrow I_C = \beta \times I_B$$

$$I_C = 50 \times (42.27 \times 10^{-6})$$

$$I_C = 2.1135 \times 10^{-3} \text{ (or) } 2.1135 mA$$

(ii) Applying KVL to the Collector ckt,

V_{CE} :-

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$= 10 - (2.1135 \times 10^{-3})(1.2 \times 10^3)$$

$$V_{CE} = 10 - 2.5362$$

$$V_{CE} = 7.4638 V$$

V_B:- iv) $V_{BE} = V_B - V_E$

$V_E = 0$

$V_{BE} = V_B$

$V_B = 0.7V$ (for Si)

V_C:- v) $V_{CE} = V_C - V_E$

$V_E = 0$

$V_C = 7.4638V$

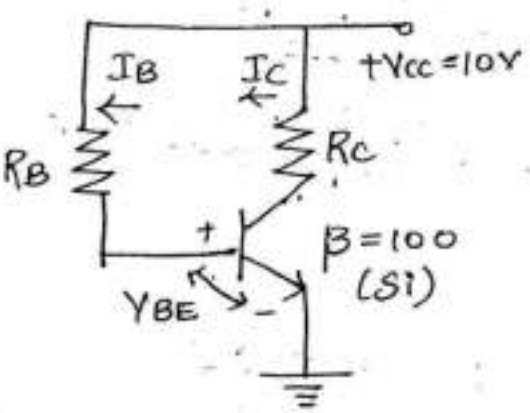
V_{BC}:- vi) $V_{BC} = V_B - V_C$

$= 0.7 - 7.4638$

$V_{BC} = -6.7638V$

Negative sign indicates Base collector junction is Reverse Biased.

10)



In the Circuit shown in fi for $R_B = 300K\Omega$ and $R_B = 150K\Omega$. calculate I_B, I_C and V_{CE}. and determine Region of operatic

s/o :-

i) $R_B = 300K\Omega$

Apply KVL at Base,

$V_{CC} - I_B R_B - V_{BE} = 0$

$I_B = \frac{V_{CC} - V_{BE}}{R_B}$

[:- V_{BE} = 0.7V for Si]

$I_B = \frac{10 - 0.7}{300 \times 10^3}$

$I_B = 0.031\,mA$

(or)

$I_B = 31\mu A$

ii) $R_B = 150K\Omega$

Apply KVL at Base,

$V_{CC} - I_B R_B - V_{BE} = 0$

$I_B = \frac{V_{CC} - V_{BE}}{R_B}$ [V_{BE}=0

$I_B = \frac{10 - 0.7}{150 \times 10^3}$

$I_B = 0.062mA$

(or)

$I_B = 62\mu A$

$I_C = \beta I_B$

$I_C = 100 \times 31\mu A$

$\boxed{I_C = 3.1mA}$

Apply KVL at collector,

$V_{CC} - I_C R_C - V_{CE} = 0$

$V_{CE} = V_{CC} - I_C R_C$

$= 10 - (3.1 \times 10^{-3}) \times (2 \times 10^3)$

$V_{CE} = 10 - 6.2$

$\boxed{V_{CE} = 3.8V}$

Comment:- $V_{CE(Active)} > V_{CE(sat)}$

Assumption that transistor is in Active Region.

$I_C = \beta I_B$

$I_C = 100 \times 62\mu A$

$\boxed{I_C = 6.2mA}$

Apply KVL at collector,

$V_{CC} - I_C R_C - V_{CE} = 0$

$V_{CE} = V_{CC} - I_C R_C$

$= 10 - (6.2 \times 10^{-3}) \times (2 \times 10^3)$

$V_{CE} = 10 - 12.4$

$\boxed{V_{CE} = -2.4V}$

Assumption that transistor is in Saturation Region

iii) Apply KVL to Base,

$V_{CC} - I_B R_B + V_{BE(sat)}$

$I_B = \frac{V_{CC} - V_{BE(sat)}}{R_B}$

$I_B = \frac{10 - 0.8}{150 \times 10^3}$ $(\because V_{BE(sat)} = 0.8)$

$I_B = 61.33\mu A$

Apply KVL to collector,

$V_{CC} - I_C R_C - V_{CE(sat)}$

$I_C = \frac{V_{CC} - V_{CE(sat)}}{R_C}$

$I_C = \frac{10 - 0.2}{2 \times 10^3}$ $(\because V_{CE(sat)} 0.2)$

$I_C = 4.9mA$

Justify, transistor in saturation, $\boxed{I_B > I_C/\beta}$

$\frac{I_C}{\beta} = \frac{4.9 \times 10^{-3}}{100} = 49\mu A$

$I_B > I_C/\beta$, Hence Verified.

Topic 2: VARIOUS BIASING METHODS FOR BJT DESIGN & STABILITY :- [BIAS STABILIZATION TECHNIQUE

(X) V.V.V.I

The Various types of Biasing circuits are

1. Fixed Bias circuit (or) Base Resistor Method.
2. Collector to Base Bias circuit
   & Modified Collector to Base Bias circuit
3. Voltage divider (or) Self Bias circuit
4. Emitter Stabilized Bias circuit

1. Fixed BIAS CIRCUIT :- STABILITY :-

(*) Derive an Expression for the Stability factor for fixed Bias Method.

(*) Draw and explain fixed Bias Method.

(*) Describe the Stability in fixed Bias.

(*) What are the Methods of BJT Biasing? [All Methods].

(*) Different types of Biasing circuit Methods.

(*) Explain the Method of Stabilizing Q-point

[M-03, 04, -05, 09, D-04, D-07, D-09 D-11]

Ans :-

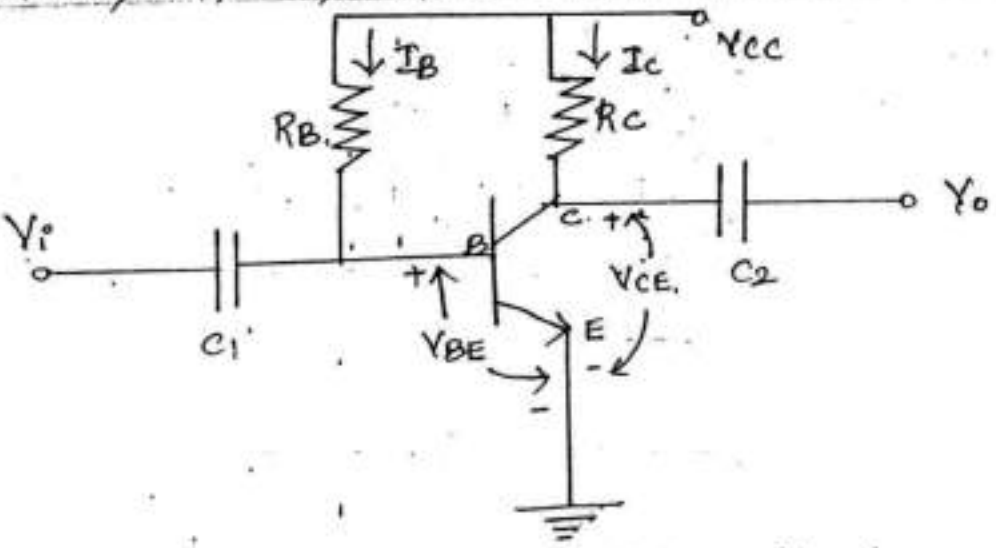


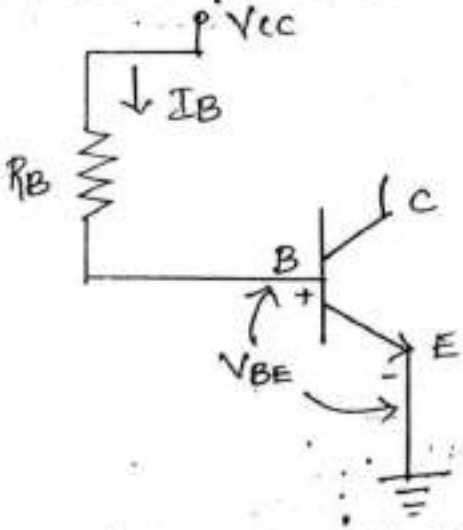
Fig (a): Fixed Bias Circuit

Def?:- (2m) → As temperature increases; collector current increases and hence base current decreases.

[Temp ↑, I_C ↑, I_B ↓]

→ R_B, R_C, V_{CC} are fixed. As they have fixed value. I_B is maintained constant. When I_C increases, so we cannot achieve the good stabilization. So, it is called as "fixed Bias".

i) Input side Loop [Base] :-



Apply Kirchoff's Voltage law on base circuit,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

I_B :-

$$V_{CC} - V_{BE} = I_B R_B$$

Base current (I_B) :-

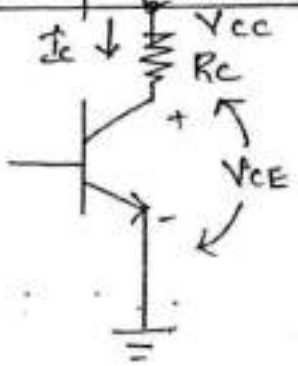
$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

R_B → Constant, V_{CC} → Constant.

V_{BE} :-

0.3 → Ge
0.7 → Si
(ON condition)

ii) Output Side Loop [Collector] :-



Apply kirchoff's Voltage law on collector circuit,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CC} - V_{CE} = I_C R_C$$

Collector current (I_C):-

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} \longrightarrow (a)$$

$$V_{CE} = V_{CC} - I_C R_C \longrightarrow (b)$$

When we take biasing circuit, the Q-pt does not lie exactly at the centre of the Active Region.

$$\beta = \frac{I_C}{I_B}$$

$$I_C = \beta I_B$$

$$V_{CE} = V_C - V_E$$

$$V_{BE} = V_B - V_E$$

$V_E = 0$ (Emitter Voltage)

$$V_{CE} = V_C$$

$$V_{BE} = V_B$$

STABILITY FACTORS:-

(2m) **Defn:-** Stability factor, which indicates degree of change in operating point due to variation in temperature.

Stability factors are,

(2m)

$S = \frac{\partial I_C}{\partial I_{CO}}$	V_{BE}, β constant
$S' = \frac{\partial I_C}{\partial V_{BE}}$	I_{CO}, β constant
$S'' = \frac{\partial I_C}{\partial \beta}$	V_{BE}, I_{CO} constant

→ Ideally, Stability factor should be perfectly zero to keep operating point stable.

→ Practically Stability factor should have value as minimum as possible.

→ Thermal Stability of a circuit is assessed by deriving a Stability factor, S.

i) Stability factor, S :- FIXED BIAS

(*) for a CE Configuration, I_c is given as,

$$\boxed{I_c = \beta I_B + I_{CEO}}$$

$$I_c = \beta I_B + (1+\beta) I_{CBO} \longrightarrow (1)$$

Diff on both sides,

$$\partial I_c = \beta \partial I_B + (1+\beta)\, \partial I_{CBO} \longrightarrow (2)$$

÷ by ∂I_c in (2)

$$\frac{\partial I_c}{\partial I_c} = \beta \frac{\partial I_B}{\partial I_c} + (1+\beta) \frac{\partial I_{CBO}}{\partial I_c}$$

$$1 = \beta \frac{\partial I_B}{\partial I_c} + (1+\beta) \frac{\partial I_{CBO}}{\partial I_c}$$

$$1 - \beta \frac{\partial I_B}{\partial I_c} = (1+\beta) \frac{\partial I_{CBO}}{\partial I_c}$$

$$\frac{\partial I_{CBO}}{\partial I_c} = \frac{1 - \beta \left[\frac{\partial I_B}{\partial I_c}\right]}{1+\beta}$$

$$\boxed{S = \frac{\partial I_c}{\partial I_{CBO}}}$$

(*) $$\boxed{S = \frac{1+\beta}{1 - \beta \left[\frac{\partial I_B}{\partial I_c}\right]}} \longrightarrow (A)$$

from eqn (A),

find $\frac{\partial I_B}{\partial I_C}$:-

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \qquad (\because V_{BE} \text{ is small})$$

$$I_B = \frac{V_{CC}}{R_B}$$

Differentiate, w.r.t. I_C

$$\frac{\partial I_B}{\partial I_C} = 0 \longrightarrow (3)$$

Sub (3) in eqn (A)

$$S = \frac{1+\beta}{1-\beta\left[\frac{\partial I_B}{\partial I_C}\right]}$$

$$= \frac{1+\beta}{1-\beta[0]}$$

$$\boxed{S = 1+\beta} \longrightarrow (4)$$

ii) Stability factor S' :-

$$\boxed{S' = \frac{\partial I_C}{\partial V_{BE}} \Big|_{I_{CO}, \beta \text{ constant}}}$$

from eqn (1) $\Rightarrow I_C = \beta I_B + (1+\beta) I_{CBO}$

$$I_C = \beta\left[\frac{V_{CC} - V_{BE}}{R_B}\right] + (1+\beta) I_{CBO}$$

$\left[\because I_B = \frac{V_{CC} - V_{BE}}{R_B}, \text{ for fixed bias}\right]$

$$I_C = \frac{\beta V_{CC}}{R_B} - \frac{\beta V_{BE}}{R_B} + (1+\beta) I_{CBO} \longrightarrow (5)$$

$I_{CBO} + \beta I_{CBO}$

Diff w.r.t. V_{BE},

$$\frac{\partial I_C}{\partial V_{BE}} = 0 - \frac{\beta}{R_B} + 0$$

$$\boxed{S' = -\frac{\beta}{R_B}} \longrightarrow (6)$$

iii) Stability factor S'' :-

$$\boxed{S'' = \frac{\partial I_C}{\partial \beta}\Big|_{V_{BE}, I_{CO} \text{ constant}}}$$

from eqn (5),

$$I_C = \frac{\beta V_{CC}}{R_B} - \frac{\beta V_{BE}}{R_B} + (1+\beta) I_{CBO}$$

Diff w.r.t. β,

$$\frac{\partial I_C}{\partial \beta} = \frac{V_{CC}}{R_B} - \frac{V_{BE}}{R_B} + I_{CBO}$$

$$= \frac{V_{CC} - V_{BE}}{R_B} + I_{CBO}$$

$$\left(\because \frac{V_{CC} - V_{CB}}{R_B} = I_B\right)$$

$$\frac{\partial I_C}{\partial \beta} = I_B + I_{CBO}$$

[$I_B >> I_{CBO}$

$I_B = \frac{I_C}{\beta}$]

$$\frac{\partial I_C}{\partial \beta} = \frac{I_C}{\beta}$$

$$\boxed{S'' = \frac{I_C}{\beta}}$$

(*) Relation between S and S' :-

$$S = 1+\beta$$

$$S' = -\frac{\beta}{R_B}$$

Multiply $(1+\beta)$ in S', $\quad \frac{-\beta(1+\beta)}{R_B(1+\beta)}$

$$S' = \frac{-\beta S}{\quad}$$

(*) Relation between S and S'' :-

$$S = 1+\beta$$

$$S'' = \frac{I_C}{\beta}$$

Multiply $(1+\beta)$ in S'' in Nr & Dr

$$S'' = \frac{I_C (1+\beta)}{\beta (1+\beta)}$$

$$S'' = \frac{I_C S}{\beta (1+\beta)}$$

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2. COLLECTOR TO BASE BIAS CIRCUIT (OR) COLLECTOR-FEEDBACK BIAS

fig :-

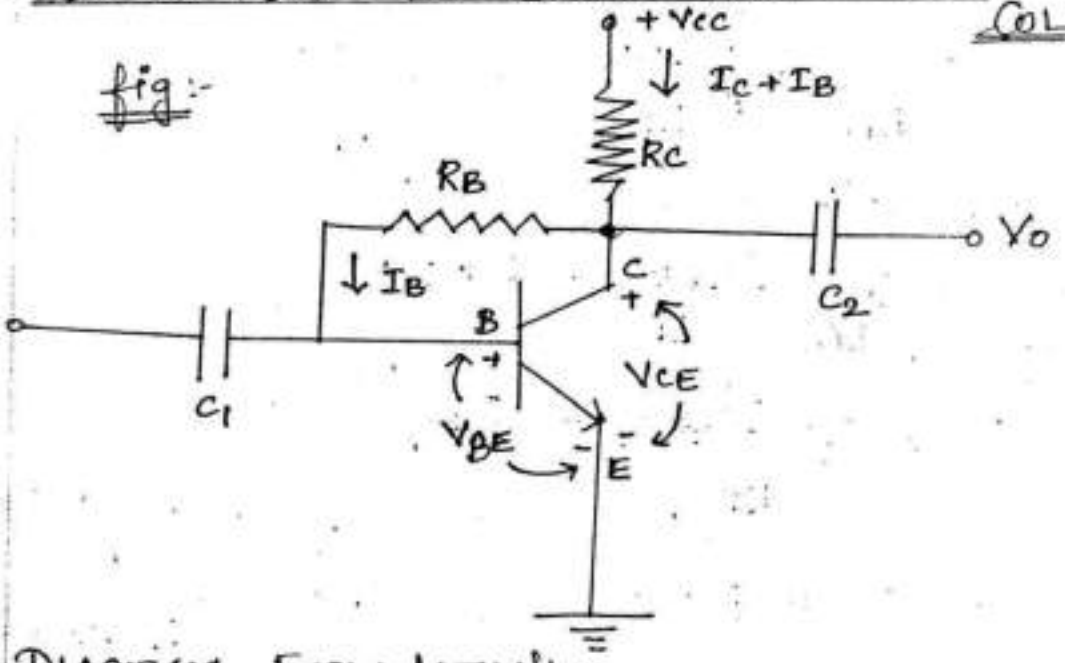


DIAGRAM EXPLANATION:-

→ It shows the d.c bias with voltage feedback.
→ It is also called the collector to base bias circuit.
→ It is an improvement over the fixed-bias
→ Biasing Resistor is connected between collector and Base of the transistor to provide a feedback path.
→ Thus, I_B flows through R_B and $(I_C + I_B)$ flows through the R_C.

(2m) Disadvantages of fixed bias :-

(*) This circuit does not provide any check on the collector current which increases with the rise in temperature i.e thermal Stability is not provided by this circuit. ∴ so operating point is not Maintained.

$$I_C = \beta I_B + I_{CEO}$$

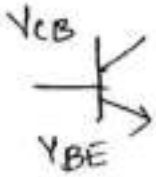
(*) Since $I_C = \beta I_B$ and I_B is already fixed, I_C depends on β which changes unit to unit and Shifts the operating point.

(*) Thus, Stabilization of operating point is very poor in the fixed bias circuit.

CIRCUIT ANALYSIS :-

→ As temperature increases, I_C increases. Result, drop across the collector resistance increases, so V_{CE} drop decreases.

→ When V_{CE} decreases, I_B also decreases – drop across decreases R_B.

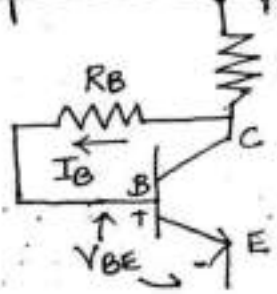


$$V_{CE} = V_{BE} + V_{CB}$$

It provides good stability.

[Temp ↑s → I_C ↑s → V_{BC} ↑s → V_{CE} ↓s → V_{CB} ↓s ← s↓ $I_B R_B$ ← When I_B ↓s I_C ↓s ←]

i) Input Side Loop :- Base circuit :-



$I_C \downarrow + I_B = I_C$

Applying Kirchoff's Voltage Law in Base circuit,

$$V_{CC} - (I_B + I_C)R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} = (I_B + I_C)R_C + I_B R_B + V_{BE}$$

$$V_{CC} = I_B R_C + I_C R_C + I_B R_B + V_{BE}$$

$$= (R_C + R_B) I_B + I_C R_C + V_{BE}$$

$$V_{CC} = (R_C + R_B) I_B + \beta I_B R_C + V_{BE} \quad (\because I_C = \beta I_B)$$

Find I_B :-

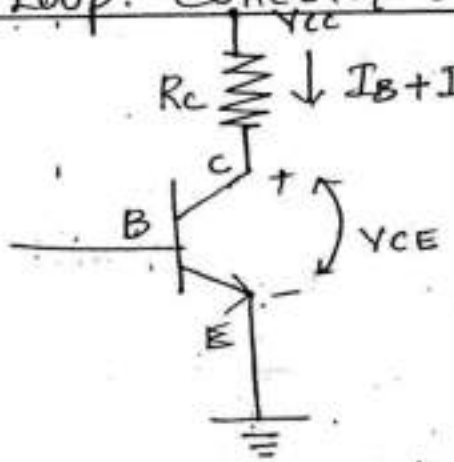
$$I_B = \frac{V_{CC} - V_{BE}}{(R_C + R_B) + \beta R_C}$$

$$= \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_C} \quad (\text{or}) \quad \frac{V_{CC} - V_{CE}}{R_B + \beta R_C} \quad (\because \beta >> 1)$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + R_C + \beta R_C}}$$

Difference only for fixed bias with this topic is the term βR_C. Thus, feedback path results in a Reflection of the resistance R_C to the input circuit.

ii) output side loop: Collector circuit



Applying KVL in the collector circuit,

$$V_{CC} - (I_C + I_B)R_C - V_{CE} = 0$$

$$V_{CC} - I_C R_C - I_B R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - (I_C + I_B) R_C$$

$$I_B = \frac{V_{CC} - V_{CE} - I_B R_C}{R_C}$$

The result is that the circuit tends to maintain a stable value of collector current, keeping the Q-point fixed.

Defn (2m) R_B appears directly across input (base) and output (collector). output is fedback to the input, and increase in collector current decreases the base current. Negative feedback exists in the circuit, so this circuit is called Voltage feedback bias circuit

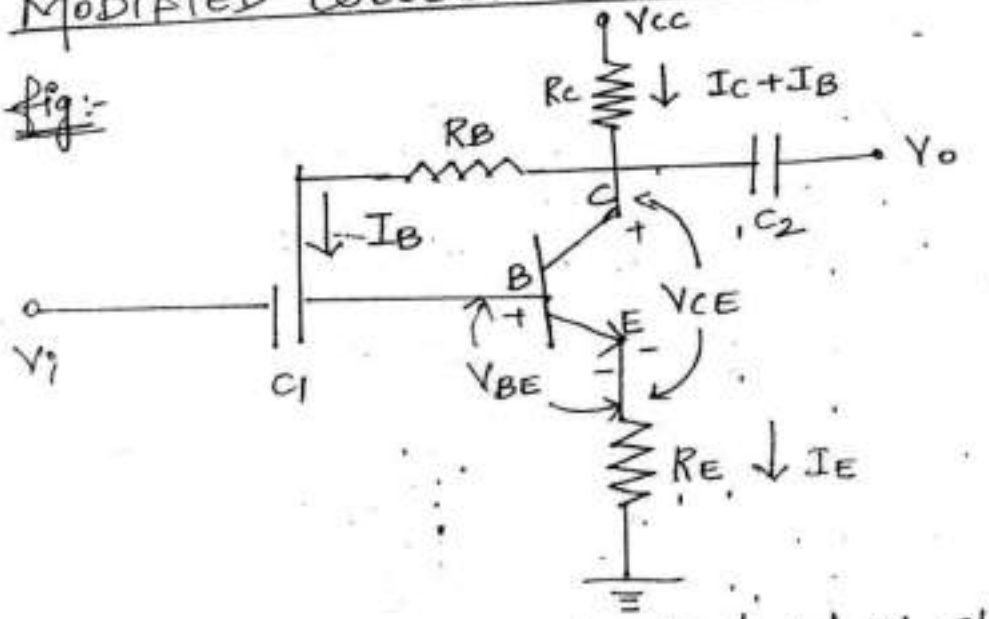
Qun: D-04 (*) prove that collector to base bias circuit is better than fixed bias circuit.

(3m) (*) Draw and Explain "collector to Base Bias" circuit

Ans: (ABOVE)

(*) MODIFIED COLLECTOR TO BASE BIAS CIRCUIT (OR) COLLECTOR TO BASE BIAS (OR) EMITTER FEEDBACK BIAS

Fig:-



→ To further improve the level of stability, the emitter resistance is connected in this circuit.

Applying KVL,

$$V_{CC} - (I_C + I_B)R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_{CC} - V_{BE} = I_B(1+\beta)R_C + I_B R_B + (1+\beta)R_E I_B$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)(R_C + R_E)}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)} \qquad \beta >> 1$$

Difference is $\beta(R_C + R_E)$ from fixed Bias.

ii) Collector circuit :-

Applying KVL,

$$V_{CC} - (I_C + I_B)R_C - V_{CE} - I_E R_E = 0$$

$$V_{CE} = V_{CC} - I_E(R_C + R_E)$$

Qun:- Explain Modified collector to Base Bias circuit.

Ans: (Above)

*) STABILITY FACTORS - COLLECTOR TO BASE BIAS :-

i)

Qun:- Derive the stability factor for the collector to Base Bi

Ans:- from the CKt,

$$V_{CC} - I_C R_C - I_B[R_C + R_B] + V_{BE} = 0$$

$$V_{CC} = I_C R_C + I_B[R_C + R_B] + V_{BE} \longrightarrow (1)$$

Diff on both sides eqn (1)

$$0 = \partial I_C R_C + \partial I_B (R_C + R_B) + 0$$

$$-\partial I_C R_C = \partial I_B (R_C + R_B)$$

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_C}{R_C + R_B}$$

Stability factor, $S = \dfrac{1+\beta}{1-\beta\left[\frac{\partial I_B}{\partial I_C}\right]}$

$$S = \frac{1+\beta}{1-\beta\left[\frac{-R_C}{R_C+R_B}\right]}$$

$$S = \frac{1+\beta}{1+\beta\left[\frac{R_C}{R_C+R_B}\right]}$$

→ Collector to Bias circuit is having lesser stability factor than for fixed bias circuit. Hence this circuit provides Better stability

ii) STABILITY FACTOR, $S' :-\ S' = \dfrac{\partial I_C}{\partial V_{BE}}$

from the CKt, (O/P)

$$V_{CC} - (I_C + I_B)R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} - I_C R_C - I_B R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} - I_C R_C - (R_C + R_B) I_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE} - I_C R_C}{R_C + R_B}$$

$$I_B = \frac{I_C}{\beta}$$

$$\frac{I_C}{\beta} = \frac{V_{CC} - I_C R_C - V_{BE}}{R_C + R_B}$$

$$\frac{I_C}{\beta} + \frac{I_C R_C}{R_C + R_B} = \frac{V_{CC} - V_{BE}}{R_C + R_B}$$

$$I_C\left[\frac{1}{\beta} + \frac{R_C}{R_C + R_B}\right] = \frac{V_{CC} - V_{BE}}{R_C + R_B}$$

$$I_C\left[\frac{R_C + R_B + R_C\beta}{\beta(R_C + R_B)}\right] = \frac{V_{CC} - V_{BE}}{R_C + R_B}$$

$$\frac{I_C}{R_C + R_B} = \frac{\beta [V_{CC} - V_{BE}]}{(R_C + R_B + \beta R_C)(R_C + R_B)}$$

$$I_C = \frac{\beta [V_{CC} - V_{BE}]}{R_B + (1+\beta) R_C}$$

Diff w.r.t. V_{BE},

$$\frac{\partial I_C}{\partial V_{BE}} = 0 - \frac{\beta}{R_B + (1+\beta) R_C}$$

$$S' = \frac{-\beta}{R_B + (1+\beta) R_C}$$

iii) STABILITY FACTOR, 'S'' :-

$$S'' = \frac{\partial I_C}{\partial \beta}$$

∴ from the ckt, (O/p)

$$V_{CC} - (I_C + I_B) R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} - V_{BE}' = (I_C + I_B) R_C - I_B R_B = 0$$

$$V_{CC} - V_{BE} = (\beta I_B + I_B) R_C - I_B R_B = 0$$

$$V_{CC} - V_{BE} = \beta I_B R_C + R_C I_B - I_B R_B$$

$$V_{CC} - V_{CE} = I_B [\beta + 1] R_C + R_B$$

$$I_B = \frac{V_{CC} - V_{CE}}{(\beta+1) R_C + R_B} \qquad (\because I_C = \beta I_B)$$

$$I_C = \frac{\beta [V_{CC} - V_{CE}]}{(\beta+1) R_C + R_B}$$

$$\left[\frac{u}{v} = \frac{vu' - uv'}{v^2}\right]$$

Diff w.r.t. β.

$$\frac{\partial I_C}{\partial \beta} = \frac{\left[(\beta+1)R_C + R_B\right]\left[V_{CC} - V_{BE}\right] - \beta\left[V_{CC} - V_{BE}\right]R_C}{\left[(\beta+1)R_C + R_B\right]^2}$$

$(V_{CC} - V_{BE})$ as common outside,

$$\frac{\partial I_C}{\partial \beta} = \frac{V_{CC} - V_{BE}\left[(\beta+1)R_C + R_B\right] - \beta R_C}{\left[(\beta+1)R_C + R_B\right]^2}$$

$$= \frac{(V_{CC} - V_{BE})(R_B + R_C + \beta R_C - \beta R_C}{\left[(\beta+1)R_C + R_B\right]^2}$$

$$= \frac{V_{CC} - V_{BE}\,(R_B + R_C)}{\left[R_B + (1+\beta)R_C\right]^2}$$

$$= \frac{V_{CC} - V_{BE}}{\left[R_B + (1+\beta)R_C\right]} \cdot \frac{\left[R_B + R_C\right]}{\left[R_B\left[1+\beta\right]R_C\right]}$$

$$\left[\because \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_C} = I_B\right]$$

$$= I_B \cdot \frac{(R_B + R_C)}{R_B + (1+\beta)R_C}$$

$$\left[\because \frac{I_C}{\beta} = I_B\right]$$

$$S'' = \frac{I_C}{\beta} \cdot \frac{\left[R_B + R_C\right]}{R_B + (1+\beta)R_C}$$

(*) Relation between S and S' :-

(2m)

$$S = \frac{1+\beta}{1+\beta\left[\frac{R_C}{R_C + R_B}\right]}$$

$$S' = \frac{-\beta}{R_B + (1+\beta)R_C}$$

$$\Rightarrow S' = -S\beta/(1+\beta)(R_C + R_B)$$

(2m) Derivation of S using S'' :-

$$S = \frac{1+\beta}{1+\beta\left[\frac{R_C}{R_C+R_B}\right]}$$

$$S'' = \frac{I_C}{\beta}\,\frac{[R_C+R_B]}{[\beta+1]R_C+R_B}$$

$$\Rightarrow S'' = \frac{I_C}{\beta}\left[\frac{S}{1+\beta}\right]$$

(2m) **Advantages of Collector-Base Bias:-**

(i) R_C must be large for Good Stabilization.

(ii) It produces Better degree of Stabilization.

∴ "If S is Small, S'' will also be Small. Thus, if we Provide Stability against I_{CO} Variations. We get Stabili against β variations also."

3. VOLTAGE DIVIDER BIAS / SELF BIAS CIRCUIT (OR) EMITTER BIAS CIRCUIT

Fig(1) :-

V.V.I

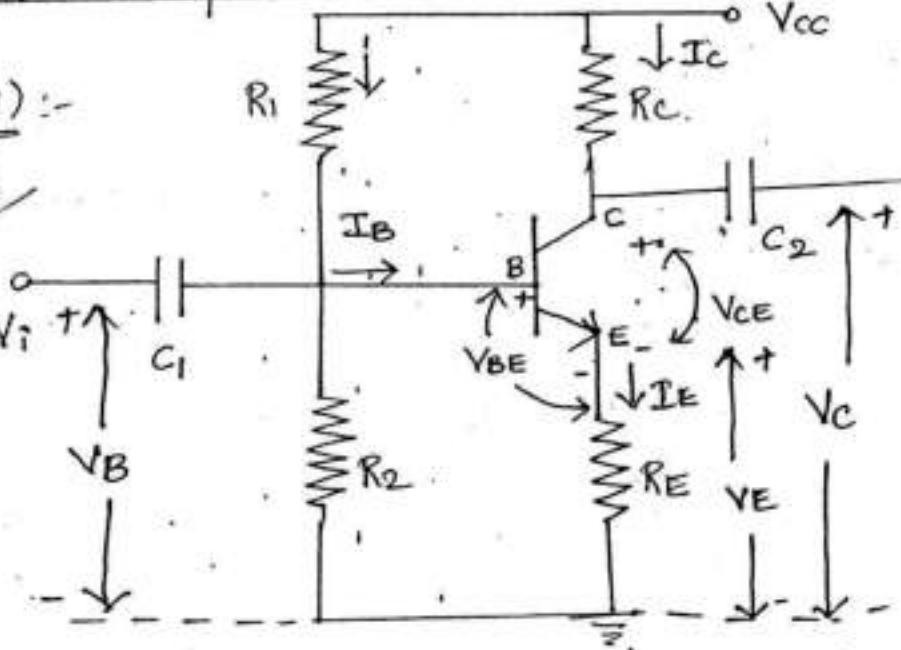


Fig: Voltage divider Bias

Diagram Explanation:-

→ It is the More Stable Biasing circuits

→ Biasing is provided by three resistors: R_1, R_2 & R

→ Resistors R_1 and R_2 acts as a potential divider (or) Voltage divider circuit.
→ If collector current increases due to change in temperature (or) change in β.
→ The emitter current I_E also increases and Voltage drop across R_E increases, reducing Voltage difference between base and emitter (V_{BE}).
→ Due to Reduction in V_{BE}, Base current I_B and hence I_C also reduces.
→ Hence, Negative feedback exists in the emitter bias circuit.
→ This Reduction in I_C compensates for original Value change in I_C.

Hint:- [Temp ↑ I_{CO} ↑ I_C ↑ Voltage drop across R_E ↑ I_E ↑ I_B ↓ I_C ↓]

CIRCUIT ANALYSIS:-

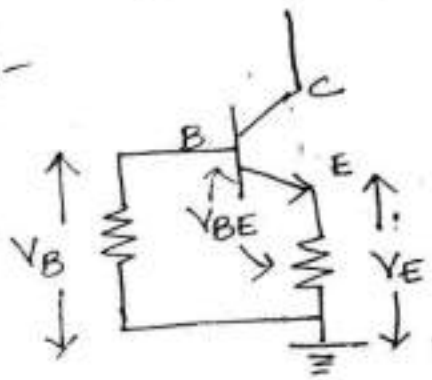
The Voltage Divider Rule, total Voltage × Particular Resistor / Sum of all Resistor

Apply Voltage divider Rule,

$$V_B = \frac{V_{CC} \cdot R_C}{R_1 + R_2} \longrightarrow (1)$$

i) Apply KVL to the Base side (input circuit)

Fig(2):-



$$V_B - V_{BE} - V_E = 0 \longrightarrow (2)$$

$$V_E = I_E R_E \longrightarrow (3)$$

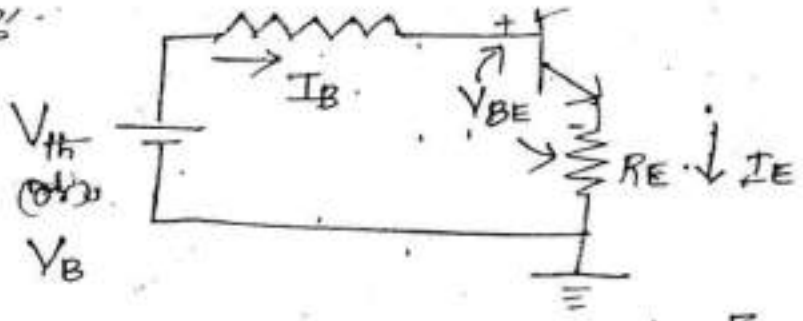
$$V_E = V_B - V_{BE} \longrightarrow (4)$$

(from eqn ②)

Equate (3) & (4).

$$I_E R_E = V_B - V_{BE}$$

$$I_E = \frac{V_B - V_{BE}}{R_E} \longrightarrow (5)$$



i) Apply KVL at the input side, [Base circuit]

$$V_{th} - R_B I_B - V_{BE} - R_E I_E = 0 \quad \text{——} (A)$$

$$V_{th} = \frac{R_2}{R_1 + R_2} \cdot V_{cc} \quad [\text{Voltage divider rule}] \quad \text{——} (B)$$

$$R_{th} = R_1 \| R_2$$

$$R_B \text{ (or) } R_{th} = \frac{R_1 R_2}{R_1 + R_2}$$

(B) in (1)

$$V_{th} = \frac{R_2}{R_1 + R_2} \cdot V_{cc}$$

$$\frac{R_2}{R_1 + R_2} \cdot V_{cc} = R_B I_B + V_{BE} + R_E I_E \qquad [\because I_E = I_C + I_B]$$

from (A) $\Rightarrow$ $V_{th} = R_B I_B + V_{BE} + R_E [I_C + I_B]$

$$V_{th} = R_B I_B + V_{BE} + I_C R_E + I_B R_E$$

$$V_{th} - V_{BE} = R_B I_B + \beta I_B R_E + I_B R_E \qquad [I_C = \beta \cdot I_B]$$

$$V_{th} - V_{BE} = I_B [R_B + \beta R_E + R_E]$$

$$\boxed{I_B = \frac{V_{th} - V_{BE}}{R_B + (1+\beta) R_E}} \longrightarrow (C)$$

Difference in $(1+\beta)R_E$ compared to other techniques.

ii) Apply KVL at the output side [collector circuit]

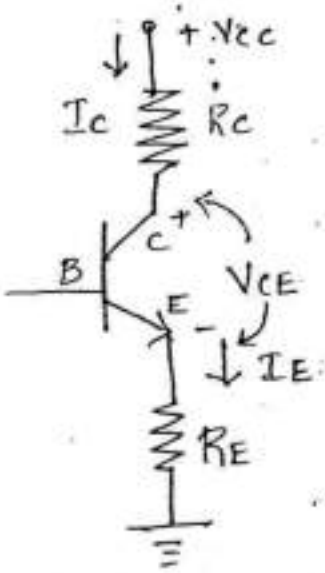
from the below fig,

$$V_{cc} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CE} = V_{cc} - I_C R_C - I_E R_E$$

(or) V_{CE}

Fig(1):-



$$V_{CE} = V_{cc} - I_C R_C - I_C R_E \qquad [\because I_E \simeq I_C$$

$$\boxed{V_{CE} = V_{cc} - I_C [R_C + R_E]}$$

$$\boxed{I_C = \frac{V_{cc} - V_{CE}}{R_C + R_E}}$$

Qun:- (*) Explain Voltage divider Bias. (self Bias)

(8m) (*) Draw the circuit of a Voltage divider Bias circuit. Explain its operation and discuss how Stabilizes against V_{BE} Changes.

(*) Draw a Voltage divider bias BJT. Derive expressions for I_{CQ} and V_{CEQ} and describe the Methods of drawing d.c. loadline on the output characteristics of transistor.

(*) Comment the performance of self bias with fixed Bias.

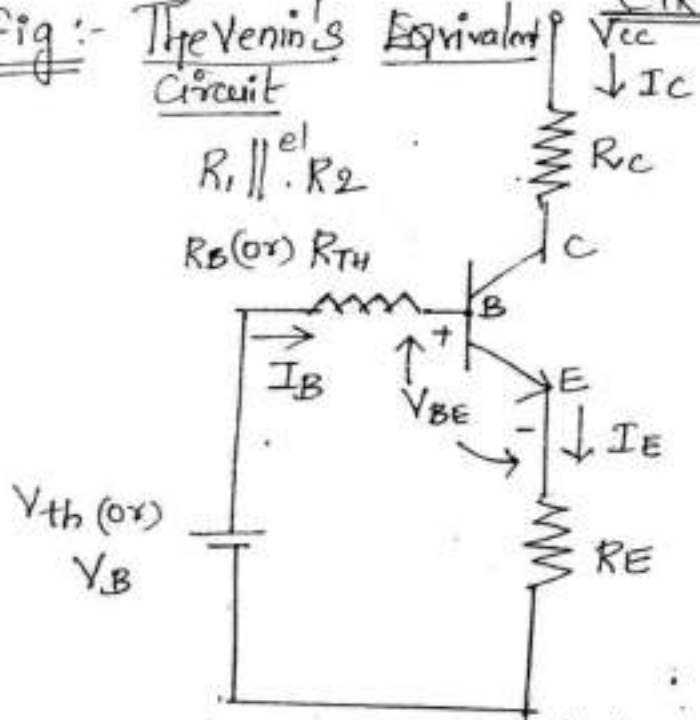
(*) Draw the circuit diagram of self bias circuit using CE configuration.

Ans:- [Above Answer]

[D-13, D-12, M-12, M-14, M-15, D-15, D-05, M-03, D-04, D-14, D-12, M-11]

*) STABILITY FACTOR - VOLTAGE DIVIDER [SELF BIAS CIRCUIT :-

Fig :- Thevenin's Equivalent Circuit



→ R_1 and R_2 is replaced by R_B (or) R_{th} and V_{th}.

→ R_B is parallel combination of R_1 and R_2.

→ V_{th} is the Thevenin's Voltage.

Apply KVL to the input (Base circuit)

$$V_{th} - I_B R_B - V_{BE} - I_E R_E = 0 \longrightarrow (1)$$

$$V_{th} - I_B R_B - V_{BE} - (I_B + I_C) R_E = 0$$

$$(\because I_E = I_B + I_C) \longrightarrow (2)$$

$$V_{th} - I_B R_B - V_{BE} - I_B R_E - I_C R_E = 0 \longrightarrow (3)$$

$$V_{th} - V_{BE} - I_C R_E = I_B R_B + I_B R_E \longrightarrow (4)$$

$$V_{th} - V_{BE} - I_C R_E = I_B [R_B + R_E]$$

$$I_B = \frac{V_{th} - V_{BE} - I_C R_E}{R_B + R_E} \longrightarrow (5)$$

Stability factor, $$S = \frac{1 + \beta}{1 - \beta \left[\frac{\partial I_B}{\partial I_C}\right]} \longrightarrow (6)$$

find $\frac{\partial I_B}{\partial I_C}$:-

$$I_B = \frac{V_{th}}{R_B+R_E} - \frac{V_{BE}}{R_B+R_E} - \frac{I_C R_E}{R_B+R_E}$$

Diff W.r.t 'Ic'

$$\frac{\partial I_B}{\partial I_C} = 0 - 0 - \frac{R_E}{R_B+R_E}$$

$$\frac{\partial I_B}{\partial I_C} = -\frac{R_E}{R_B+R_E} \longrightarrow (7)$$

Sub (7) in eqn (6)

$$S = \frac{1+\beta}{1-\beta\left[\frac{-R_E}{R_B+R_E}\right]} \longrightarrow (8)$$

$$\boxed{S = \frac{1+\beta}{1+\beta\left[\frac{R_E}{R_B+R_E}\right]}}$$

$$= \frac{1+\beta}{\left(\frac{R_B+R_E+\beta R_E}{R_B+R_E}\right)}$$

$$S = \frac{(1+\beta)(R_B+R_E)}{R_B+R_E+\beta R_E} \longrightarrow (9)$$

÷ each terms by R_E

$$S = \frac{(1+\beta)\left(1+\frac{R_B}{R_E}\right)}{\frac{R_B}{R_E}+1+\beta} \longrightarrow (10)$$

$$S = \frac{(1+\beta)\left(1+\frac{R_B}{R_E}\right)}{(1+\beta)+\frac{R_B}{R_E}} \quad \left[\because \frac{R_B}{R_E} \text{ is } <<< 1\right] \longrightarrow (11)$$

$$S = \frac{(1+\beta)(1)}{(1+\beta)} \qquad \boxed{S=1} \longrightarrow (12)$$

i) S' :-

$$\boxed{S' = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{I_{CO}, \beta \text{ are constant}}} \longrightarrow (13)$$

General expression, $I_C = \beta I_B + (1+\beta) I_{CO}$ $\longrightarrow (14)$

$$I_C = \beta I_B \longrightarrow (15)$$

$$I_C = \beta \cdot I_B$$

from eqn (5) $\Rightarrow$ $I_B = \dfrac{V_{th} - V_{BE} - I_C R_E}{R_B + R_E}$

$$I_C = \beta \cdot \left[\frac{V_{th} - V_{BE} - I_C R_E}{R_B + R_E}\right] \longrightarrow (16)$$

$$\frac{I_C}{\beta} = \frac{V_{th} - V_{BE} - I_C R_E}{R_B + R_E}$$

$$\frac{I_C}{\beta} = \frac{V_{th} - V_{BE}}{R_B + R_E} - \frac{I_C R_E}{R_B + R_E} \longrightarrow (17)$$

$$\frac{I_C}{\beta} + \frac{I_C R_E}{R_B + R_E} = \frac{V_{th} - V_{BE}}{R_B + R_E}$$

$$I_C\left[\frac{1}{\beta} + \frac{R_E}{R_B + R_E}\right] = \frac{V_{th} - V_{BE}}{R_B + R_E}$$

$$I_C\left[\frac{R_B + R_E + \beta R_E}{\beta (R_B + R_E)}\right] = \frac{V_{th} - V_{BE}}{R_B + R_E}$$

$$I_C = \frac{(V_{th} - V_{BE})(\beta(R_B + R_E))}{(R_B + R_E)(R_B + R_E + \beta R_E)}$$

$$I_C = \frac{\beta (V_{th} - V_{BE})}{R_B + R_E(1+\beta)} \longrightarrow (18)$$

$$I_C = \frac{\beta V_{th}}{R_B + R_E(1+\beta)} - \frac{V_{BE}\beta}{R_B + R_E(1+\beta)} \longrightarrow (19)$$

$$S' = \frac{\partial I_C}{\partial V_{BE}}$$

D.W.r.t. V_{BE} on eqn (19).

$$\frac{\partial I_C}{\partial V_{BE}} = 0 - \frac{\beta}{R_B + R_E(1+\beta)}$$

$$\boxed{S' = \frac{-\beta}{R_B + R_E(1+\beta)}} \longrightarrow (20)$$

iii) S'' :-

$$\boxed{S'' = \frac{\partial I_C}{\partial \beta}\Big|_{I_{CO}, V_{BE} \to \text{constant}}} \longrightarrow (21)$$

eqn (19) $\Rightarrow I_C = \dfrac{\beta[V_{th} - V_{BE}]}{R_B + R_E(1+\beta)}$

Diff w.r.t I_C with β. $\quad \frac{u}{v} = \frac{vu' - uv'}{v^2}$

$$\frac{\partial I_C}{\partial \beta} = \frac{R_B + R_E(1+\beta)(V_{th} - V_{BE}) - \beta(V_{th} - V_{BE})(R_E)}{[R_B + R_E(1+\beta)]^2}$$

$$\frac{\partial I_C}{\partial \beta} = \frac{(V_{th} - V_{BE})[R_B + R_E + \beta R_E - \beta R_E]}{[R_B + R_E(1+\beta)]^2}$$

$$= \frac{(V_{th} - V_{BE})(R_B + R_E)}{[R_B + R_E(1+\beta)]^2}$$

$$\frac{\partial I_C}{\partial \beta} = \frac{(V_{th} - V_{BE})(R_B + R_E)}{[R_B + R_E(1+\beta)][R_B + R_E(1+\beta)]} \longrightarrow (22)$$

on (c) $\Rightarrow I_B = \dfrac{V_{th} - V_{BE}}{[R_B + R_E(1+\beta)]}$

$$\frac{\partial I_C}{\partial \beta} = \frac{I_B \cdot (R_B + R_E)}{[R_B + R_E(1+\beta)]} \longrightarrow (23)$$

$$\Delta I_B = \frac{\Delta I_C}{\beta} \longrightarrow (24)$$

Sub (24) in eqn (23)

$$\frac{\partial I_C}{\partial \beta} = \frac{I_C}{\beta} \cdot \frac{(R_B + R_E)}{R_B + R_E(1+\beta)} \longrightarrow (25)$$

x'y l ÷ by $(1+\beta)$

$$S'' = \frac{I_C}{\beta} \cdot \frac{(1+\beta)}{(1+\beta)} \frac{(R_B+R_E)}{[R_B+R_E(1+\beta)]}$$

from eqn (9), $S = \frac{(1+\beta)(R_B+R_E)}{R_B+R_E(1+\beta)}$

$$\boxed{S'' = \frac{I_C}{\beta} \cdot \frac{S}{1+\beta}}$$

Advantages of Voltage divider Bias:-

m) (i) Stability factor 'S' for Voltage divider bias is less compared to other Biasing circuits. It is known as Self Biasing circuits.

(ii) If self Bias circuit, when R_B/R_E is small, $S = 1$ which provides good stability

(iii) It is More Stable, popular for stability.

Qun: (*) Derive the stability factor of self bias circuit of BJT.

m/16m (*) Derive all stability factors, S, S', S'' for Voltage divide bia

(*) Derive stability factor $\frac{\partial I_C}{\partial h_{FE}}(\beta)$ in self bias circuit. What are the design considerations to make stabili factor independent of h_{FE} variation.

(*) Prove that Self Bias of Stability factors.

Ans- [Above Answer]. [D-04, D-05, D-02, D-14, D-13, M-13, M-12, D-11, M-15, D-15, M-14]

PROBLEMS [FIXED BIAS/SELF BIAS[Voltage divider bias] COLLECTOR TO BASE BIAS]

11) In fixed Bias Method, a Si transistor with $\beta = 100$ $V_{cc} = 6V$, $R_C = 3K\Omega$, $R_B = 530K\Omega$. Draw the DC LoadLin determine the operating point. What is the Stability fa

Soln:-

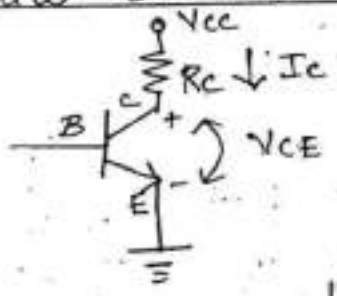
Given: $\beta = 100$

$R_C = 3K\Omega$

$R_B = 530K\Omega$

$V_{cc} = 6V$

i) To Draw DC Load Line:-



$V_{cc} - I_C R_C - V_{CE} = 0$

$6 - I_C(3K) - V_{CE} = 0 \rightarrow (1)$

a) To find V_{CE}:- $(I_C = 0)$

$(1) \Rightarrow 6 - 0 - V_{CE} = 0$

$V_{CE} = 6V$

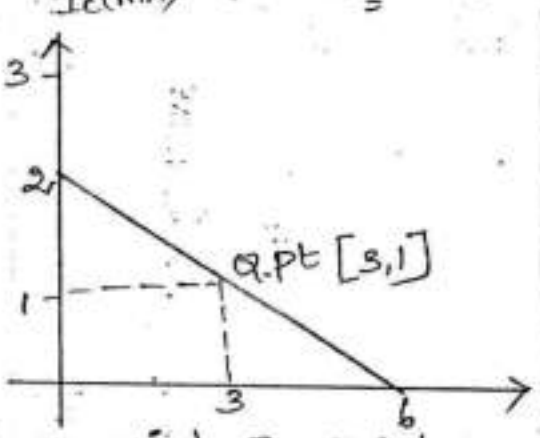
b) To find I_C:- $(V_{CE} = 0)$

$(1) \Rightarrow 6 - I_C(3K) - 0$

$I_C = \frac{6}{3 \times 10^3}$

$I_C = 2 \times 10^{-3}$

$I_C = 2mA$



ii) To Find Q.-point :-

Input side, $I_B = \frac{V_{cc} - V_{BE}}{R_B} \Rightarrow \frac{6 - 0.7}{530 \times 10^3}$ $(V_{BE} = 0.7V)$

$= \frac{5.3}{530 \times 10^3} \Rightarrow 1 \times 10^{-5}$

$I_B = 10\mu A$

output side, $V_{CE} = V_{cc} - I_C R_C$

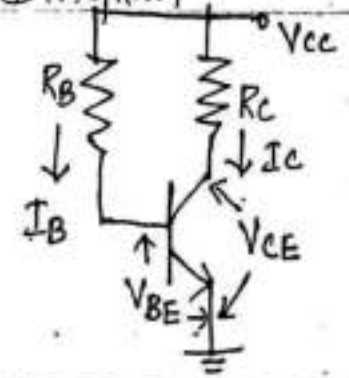
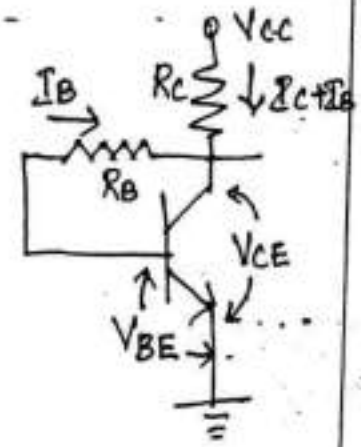
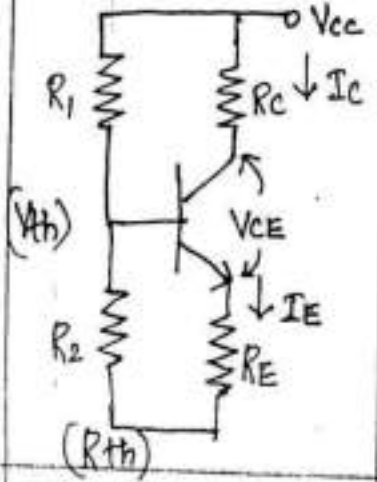
$V_{CE} = 6 - (1 \times 10^{-3})(3 \times 10^3)$

$V_{CE} = 3V$

iii) Stability factor:-

$S = 1 + \beta$ [for fixed Bias]

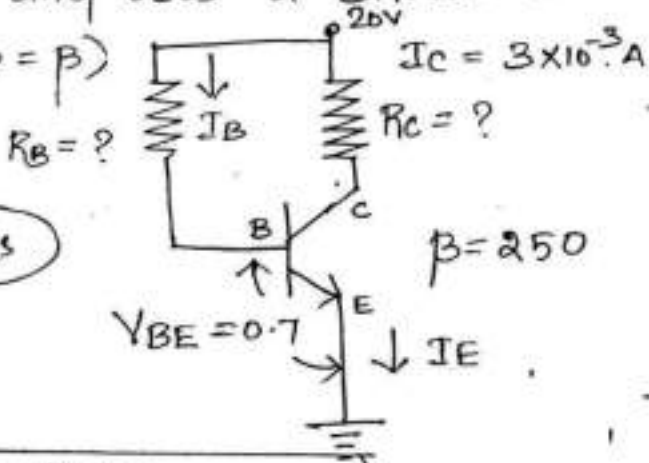
$S = 1 + 100 \Rightarrow S = 101$

BIASING CIRCUIT	CIRCUIT DIAGRAM	$I_{CQ} = \beta I_{BQ}$		LINE	$S = \frac{\partial I_C}{\partial I_{CO}}$	$S' = \frac{\partial I_C}{\partial V_{BE}}$	$S'' = \frac{\partial I_C}{\partial \beta}$
FIXED BIAS		$I_B = \frac{V_{CC} - V_{BE}}{R_B}$	$V_{CE} = V_{CC} - I_C R_C$	$I_C = 0,\ V_{CE} = V_{CC}$ $V_{CE} = 0,\ I_C = \frac{V_{CC}}{R_C}$	$S = 1+\beta$	$S' = \frac{-\beta}{R_B}$	$S'' = \frac{I_C}{\beta}$
COLLECTOR TO BASE BIAS		$I_B = \frac{V_{CC} - V_{BE}}{R_B + R_C(1+\beta)}$	$V_{CE} = V_{CC} - I_C R_C$	$I_C = 0,\ V_{CE} = V_{CC}$ $V_{CE} = 0,\ I_C = \frac{V_{CC}}{R_C}$	$S = \frac{1+\beta}{1+\beta\left[\frac{R_C}{R_B+R_C}\right]}$	$S' = \frac{-\beta}{R_B + (1+\beta)R_C}$	$S'' = \frac{I_C}{\beta} \cdot \frac{R_B + R_C}{R_B + R_C(1+\beta)}$
VOLTAGE DIVIDER BIAS (OR) SELF BIAS		$I_B = \frac{V_{th} - V_{BE}}{R_B + R_E(1+\beta)}$	$V_{CE} = V_{CC} - I_C(R_C + R_E)$	$I_C = 0,\ V_{CE} = V_{CC}$ $V_{CE} = 0,\ I_C = \frac{V_{CC}}{R_C + R_E}$	$S = \frac{1+\beta}{1+\beta\left[\frac{R_E}{R_B+R_E}\right]}$	$S' = \frac{-\beta}{R_B + R_E(1+\beta)}$	$S'' = \frac{I_C}{\beta} \cdot \frac{S}{1+\beta}$

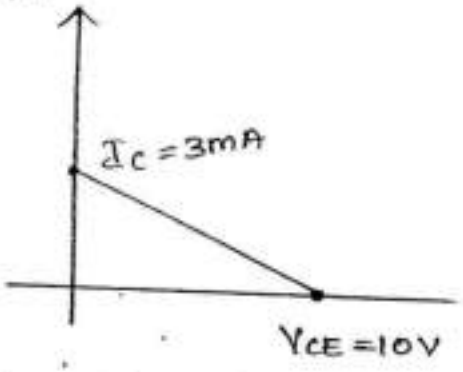
Problems Continuation,

12) Design a Fixed Bias circuit to have operating Point of (10V, 3mA). The circuit is supplied with 20V and uses a Silicon transistor of $h_{fe} = 25$ ($h_{fe} = \beta$)

Soln :-



Fixed Bias



Formula :-

$$I_C = \beta I_B$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$V_{CE} = V_{CC} - I_C R_C$$

Find :- $R_C = ?$ $R_B = ?$

Soln :- i) R_C :-

$$V_{CE} = V_{CC} - I_C R_C$$

$$R_C = \frac{V_{CC} - V_{CE}}{I_C}$$

$$R_C = \frac{20 - 10}{3 \times 10^{-3}}$$

$$R_C = \frac{10 \times 10^3}{3}$$

$$R_C = 3.33 \times 10^3$$

$$R_C = 3.33 K\Omega$$

ii) R_B :-

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

$$R_B = \frac{V_{CC} - V_{BE}}{(I_C/\beta)_B}$$

$$R_B = \frac{20 - 0.7}{((3 \times 10^{-3})/250)}$$

$$R_B = \frac{250(20 - 0.7)}{3 \times 10^{-3}}$$

$$R_B = \frac{4825}{3 \times 10^{-3}}$$

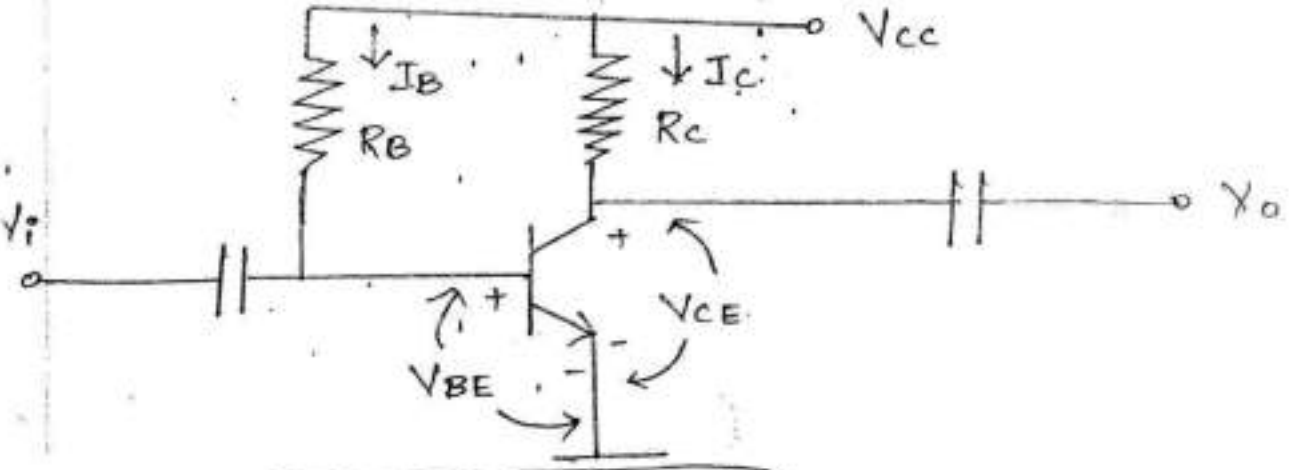
$$R_B = 1608333.333$$

Ans :-

$R_C = 3.33 K\Omega$

$R_B = 1.6 M\Omega$

3) Design the circuit shown in the Fig. Given Q-point values are to be $I_{CQ} = 1mA$, $V_{CEQ} = 6V$ Assume that $V_{cc} = 10V$, $\beta = 100$, $V_{BE}(ON) = 0.7V$ (31)



This is fixed Bias circuit

Formula:-

$$I_C = \beta I_B$$

$$I_B = \frac{V_{cc} - V_{BE}}{R_B}$$

$$V_{ce} = V_{cc} - I_C R_C$$

Find:- $R_C = ?$ $R_B = ?$

Soln:-

i) To Find R_C:-

$$V_{CE} = V_{cc} - I_C R_C$$

$$R_C = \frac{V_{cc} - V_{CE}}{I_C}$$

$$R_C = \frac{10 - 6}{1 \times 10^{-3}}$$

$$R_C = 4 \times 10^3$$

$$R_C = 4K\Omega$$

ii) To Find R_B:-

$$I_B = \frac{V_{cc} - V_{BE}}{R_B}$$

$$R_B = \frac{V_{cc} - V_{BE}}{I_B}$$

$$R_B = \frac{10 - 0.7}{(I_C/\beta)}$$

$$R_B = \frac{100[9.3]}{1 \times 10^{-3}}$$

$$R_B = 930 \times 10^3$$

$$R_B = 930k\Omega$$

Ans:-

$R_C = 4K\Omega$

$R_B = 930K\Omega$

14) In a CE Configuration, Germanium transistor amplifier circuit the bias is provided by self b

The various parameters are $V_{cc} = 16V$, $R_C = 3K\Omega$, $R_E = 2K\Omega$, $R_1 = 56K\Omega$, $R_2 = 20K\Omega$, $\alpha = 0.985$. Determine
(i) the co-ordinates of operating point.
(ii) Stability factor S.

Hint :- (Self Bias)

Formula :- $I_C = \frac{\beta [V_{th} - V_{BE}]}{R_B + (1+\beta) R_E}$, $\beta = \frac{\alpha}{1-\alpha}$

R_B (or) $R_{th} = \frac{R_1 R_2}{R_1 + R_2}$

$I_E = I_C + I_B$

$V_{th} = \frac{R_2 . V_{cc}}{R_1 + R_2}$

$V_{CE} = V_{cc} - I_C [R_C + R_E]$

$S = \frac{[R_B + R_E][1+\beta]}{R_B + (1+\beta) R_E}$ (or) $S = \frac{1+\beta}{1+\beta \left[\frac{R_E}{R_B + R_I}\right.}$

Soln :- i) Co-ordinate of operating point :- (I_C, V_{CE})

a) To Find I_C :-

$$I_C = \frac{\beta [V_{th} - V_{BE}]}{R_B + [1+\beta] R_E}$$

Want to find β, V_{th}, R_B :-

β :- $\beta = \frac{\alpha}{1-\alpha}$

$\beta = \frac{0.985}{1-0.985}$

$\beta = \frac{0.985}{0.015}$

$\beta = 65.667$

R_{th} (or) R_B :-

$R_B = \frac{R_1 R_2}{R_1 + R_2}$

$= \frac{(56 \times 10^3)(20 \times 10^3)}{(56 \times 10^3) + (20 \times 10^3)}$

$R_B = 14736.842\ \Omega$

V_{th} :- $V_{th} = \frac{R_2}{R_1 + R_2} . V_{cc}$

$= (20 \times 10^3)(16) / (56 \times 10^3) + (20 \times 10^3)$

$= \frac{320}{76}$

$V_{th} = 4.210V$

Sub β, V_{th}, R_B in I_C

$$I_C = \frac{\beta [V_{th} - V_{BE}]}{R_B + (1+\beta) R_E}$$

[$\because V_{BE} = 0.3V$ (Ge. Transis

$$= \frac{65.667 [4.210 - 0.3]}{14736.842 + [1 + 65.667](2 \times 10^3)}$$

$$= \frac{256.757}{148070.842}$$

$$= 1.734 \times 10^{-3}$$

$$I_C = 1.734mA$$

b) To Find V_{CE} :-

$$V_{CE} = V_{cc} - I_C [R_C + R_E]$$

$$V_{CE} = 16 - (1.734 \times 10^{-3}) [3 \times 10^3 + 2 \times 10^3]$$

$$V_{CE} = 16 - 1.734 \times 10^{-3} \times 10^3 [3+2]$$

$$= 16 - 1.734 [5]$$

$$V_{CE} = 7.33V$$

$\therefore$ The Co-ordinates of operating point are,

$$Q [1.734mA, 7.33V]$$

(ii) Stability Factor 'S' :-

$$S = \frac{[R_B + R_E][1+\beta]}{R_B + [1+\beta] R_E} \quad (or) \quad \frac{1+\beta}{1+\beta \left[\frac{R_E}{R_B + R_E}\right]}$$

$$= \frac{[14736.842 + 2 \times 10^3][1 + 65.667]}{14736.842 + [1 + 65.667](2 \times 10^3)}$$

$$= \frac{(16736.842)(66.667)}{14736.842 + 133334}$$

$$S = 7.53$$

15) A series Amplifier with Voltage divider bias is designed to establish Q-point at $V_{CE} = 12V$, $I_C = 2mA$ and Stability factor $S = 5.1$ if $V_{CC} = 24V$ $V_{BE} = 0.7V$, $\beta = 50$ and $R_C = 4.7K\Omega$. Determine the values of resistors R_E, R_1 and R_2.

Hint:- (Voltage divider Bias)

Formula:- i) $V_{CE} = V_{CC} - I_C(R_C + R_E)$, Find R_E

ii) $S = \frac{[R_B + R_E][1+\beta]}{R_B + R_E[1+\beta]}$, Find R_B, $R_B = R_1 \| R_2$

$$R_B = \frac{R_1 R_2}{R_1 + R_2}$$

Soln:- i) To Find R_E:-

$$V_{CE} = V_{CC} - I_C[R_C + R_E]$$

$$12 = 24 - 2\times10^{-3}[4.7\times10^{3} + R_E]$$

$$12 = 24 - 9.4 - 2\times10^{-3} R_E$$

$$2\times10^{-3} R_E = 24 - 9.4 - 12$$

$$R_E = \frac{24 - 9.4 - 12}{2\times10^{-3}}$$

$$R_E = 1.3\times10^{3}$$

$$R_E = 1.3K\Omega$$

Given

$V_{CE} = 12V$
$V_{CC} = 24V$
$I_C = 2mA = 2\times10^{-3}A$
$R_C = 4.7K\Omega = 4.7\times10^{3}$

(ii) To Find R_1 and R_2 (R_B):-

$$S = \frac{[R_B + R_E][1+\beta]}{R_B + [1+\beta]R_E}$$

$$5.1 = \frac{[R_B + 1.3\times10^{3}][1+50]}{R_B + [1+50](1.3\times10^{3})}$$

Given

$\beta = 50$
$S = 5.1$
$R_E = 1.3K$
$= 1.3\times$

$$5.1 = \frac{(R_B + 1.3\times10^{-3})(51)}{R_B + 66300}$$

$$5.1R_B + 338130 = 51R_B + 66300$$

$$5.1R_B - 51R_B = 66300 - 338130$$

$$-45.9R_B = -271830$$

$$R_B = \frac{271830}{45.9}$$

$$\boxed{R_B = 5922.22\,\Omega}$$

Find R_1 and R_2 :-

$$R_B = R_1 \parallel R_2$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2} \longrightarrow (B)$$

$[\because R_2 = 0.1\beta RE]$

$$R_2 = 0.1 \times 50 \times 1.3\times10^{3}$$

$$\boxed{R_2 = 6500\,\Omega} \longrightarrow (A)$$

Sub (A) in (B)

$$5922.22 = \frac{R_1(6500)}{R_1 + 6500}$$

$$5922.22R_1 + 5922.22(6500) = 6500R_1$$

$$38494430 = 6500R_1 - 5922.22R_1$$

$$38494430 = 577.78R_1$$

$$R_1 = \frac{38494430}{577.781}$$

$$R_1 = 66622.71$$

$$\boxed{R_1 = 6.66\,K\Omega}$$

Ans :-

$R_E = 1.3K\Omega$

$R_B = 5922.22\,\Omega$

$R_1 = 6.66K\Omega$, $R_2 = 6500\Omega$

16) An NPN transistor, if $\beta = 50$ is used in series and circuit with $V_{cc} = 10V$ and $R_c = 2K\Omega$. The Bias is obtained by connecting $100K\Omega$ resistor from collector to Base. Find the 'Q-point and Stability Factor S

Hint:- **Collector to Base circuit**

formula:-

$$I_c = \frac{\beta[V_{cc} - V_{BE}]}{\beta R_c + R_B + R_c}$$

$$V_{CE} = V_{cc} - I_c R_c$$

$$S = \frac{1 + \beta[R_B + R_c]}{R_B + (1+\beta)R_c}$$

Given :-

$V_{cc} = 10V$

$R_c = 2K\Omega = 2 \times 10^3 \Omega$

$\beta = 50$

$V_{BE} = 0.7V$

Soln :- i) Q-point :- $[V_{CE}, I_c]$

a) Find I_c :-

$$I_c = \frac{\beta[V_{cc} - V_{BE}]}{\beta R_c + R_B + R_c}$$

$$= \frac{50[10 - 0.7]}{50[2\times10^3] + (100\times10^3) + (2\times10^3)}$$

$$= \frac{465}{(100\times10^3) + (100\times10^3) + (2\times10^3)}$$

$$= 2.32 \times 10^{-3}$$

$$I_c = 2.32mA$$

b) Find V_{CE} :-

$$V_{CE} = V_{cc} - I_c R_c$$

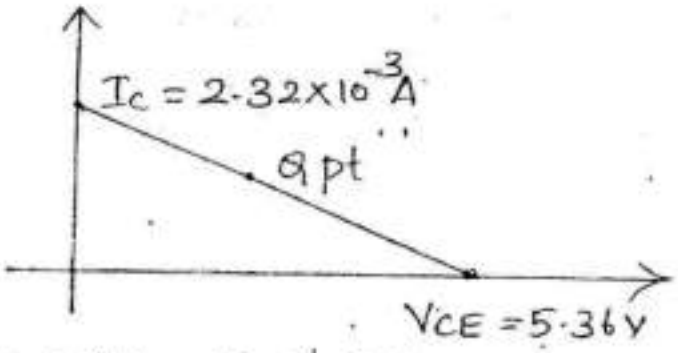
$$= 10 - (2.32\times10^{-3})(2\times10^3)$$

$$= 10 - 2.32 \times 2$$

$$= 10 - 4.64$$

$$V_{CE} = 5.36V$$

$\therefore$ Q Point is $(V_{CEQ}, I_{CQ}) \Rightarrow (5.36V, 2.32mA)$



i) Stability factor 'S' :-

$$S = \frac{1+\beta[R_B+R_C]}{R_B+[1+\beta]R_C}$$

$$= \frac{1+50[100\times10^3 + 2\times10^3]}{100\times10^3 + [1+50](2\times10^3)}$$

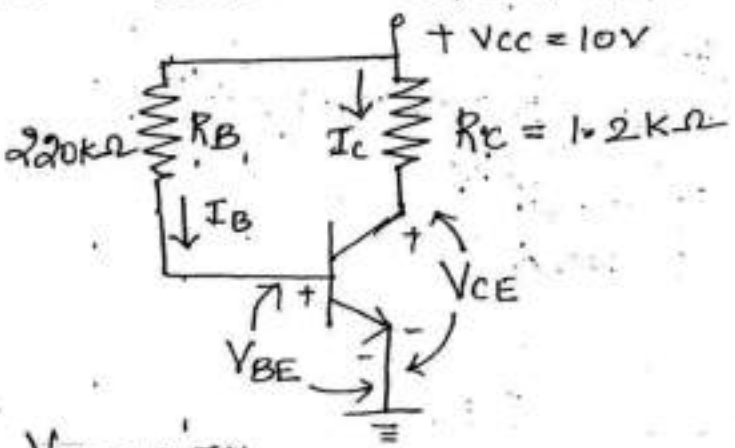
$$= \frac{1+50[102\times10^3]}{100\times10^3 + 102\times10^3}$$

$$= \frac{1+5100\times10^3}{(100+102)\times10^3}$$

$$S = 25.75$$

---

(7) In the circuit, shown in figure, where $V_{CC} = 10V$ $R_B = 220K\Omega$. calculate I_B, I_C, V_{CE}.



Assume $V_{BE} = 0.7V$

$\beta = 50$

Hint:- (fixed bias circuit)

Formula:- i) $I_B = \frac{V_{CC} - V_{BE}}{R_B}$

ii) $I_C = \beta I_B$

iii) $V_{CE} = V_{CC} - I_C R_C$

Soln :- (i) Find I_B :-

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \quad \ldots 1$$

$$= \frac{10 - 0.7}{(220 \times 10^3)}$$

$$= \frac{9.3}{220000}$$

$$I_B = 42.27 \times 10^{-6}$$

$$\boxed{I_B = 42.27 \mu A}$$

(ii) Find I_C :-

$$I_C = \beta I_B$$

$$I_C = 50 \times 42.27 \times 10^{-6}$$

$$I_C = 2.1135 \times 10^{-3}$$

$$\boxed{I_C = 2.1135 mA}$$

(iii) Find V_{CE} :-

$$V_{CE} = V_{CC} - I_C R_C$$

$$= 10 - (2.1135 \times 10^{-3})(1.2 \times 10^3)$$

$$V_{CE} = 7.4638 V$$

Ans :-

$$\boxed{\begin{aligned} I_B &= 42.27 \mu A \\ I_C &= 2.1135 mA \\ V_{CE} &= 7.4638 V \end{aligned}}$$

(18) Estimate the value of the Resistor in the Fixed Biasing circuit. Using the Following Specificatio

$V_{CE} = 4.4V$, $V_{BE} = 0.7V$, $I_{CO} = 9mA$

$\beta = 115$, $V_{CC} = 9V$

Find R_C, I_B, R_B ?

Formula:- i) $V_{CE} = V_{CC} - I_C R_C$

ii) $I_C = \beta I_B$

iii) $I_B = \frac{V_{CC} - V_{BE}}{R_B}$

Soln :- i) Find R_C :-

$$V_{CE} = V_{CC} - I_C R_C$$

$$R_C = \frac{V_{CC} - V_{CE}}{I_C}$$

$$R_C = \frac{9 - 4.4}{(9 \times 10^{-3})}$$

$$R_C = \frac{4.6 \times 10^3}{9}$$

$$= 0.51111 \times 10^3$$

$$R_C = 511.11\ \Omega$$

ii) Find I_B :-

$$\beta = \frac{I_C}{I_B}$$

$$I_B = \frac{I_C}{\beta}$$

$$I_B = \frac{9 \times 10^{-3}}{115}$$

$$I_B = 0.07826 \times 10^{-3}$$

$$I_B = 78.26 \times 10^{-6} A$$

$$I_B = 78.26\ \mu A$$

iii) Find R_B :-

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

$$R_B = \frac{9 - 0.7}{78.26 \times 10^{-6}}$$

$$R_B = \frac{8.3}{78.26} \times 10^6$$

$$R_B = 0.106056 \times 10^6$$

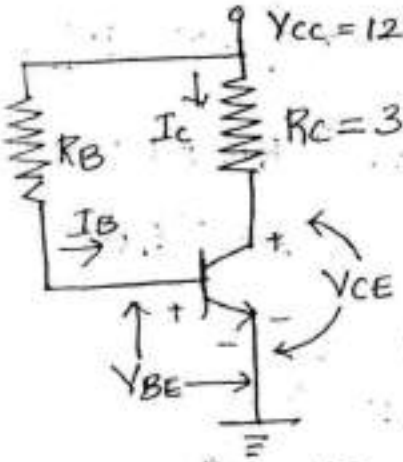
$$R_B = 106 \times 10^3\ \Omega$$

$$R_B = 106\ k\Omega$$

Ans:- $R_C = 511.11\ \Omega$ $\quad I_B = 78.26\ \mu A$

$R_B = 106\ k\Omega$

(19) M-08 (Sm)



$I_B = 0.3mA$
$= 0.3 \times 10^{-3} A$
$\beta = 100$
$V_{CE} = 6V$
$V_{BE} = 0.7V$

Determine the Bias transistori R_B for fixed Bi and collector to Baise Bias, and compare the Stability factor S for both of them.

Hint:- I. (FIXED BIAS)

(i) Find R_B :-

$V_{cc} = V_{BE} + I_B R_B$

$R_B = \frac{V_{cc} - V_{BE}}{I_B}$

$R_B = \frac{12 - 0.7}{(0.3 \times 10^{-3})}$

$R_B = 37.67 K\Omega$

(ii) Stability Factor 'S' :-

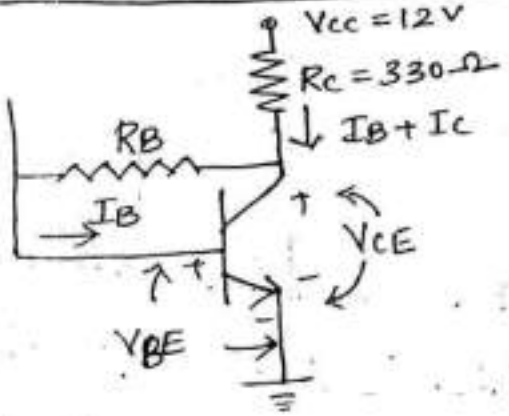
$S = 1 + \beta$

$S = 1 + 100$

$S = 101$

Ans :- $R_B = 37.67 K\Omega$
$S = 101$

II. (Collector to Base Bias)



(i) Find R_B :-

$V_{cc} - (I_B + I_c) R_C - I_B R_B - V_{BE} = 0$

$I_c = \beta \times I_B$

$= 100 \times 0.3 \times 10^{-3}$, $I_c = 0.03A$

$V_{CC} = [(0.3 \times 10^{-3}) + (0.03)] 330 + [0.3 \times 10^{-3}] R_B + 0.7$

(3)

$12 = 9.99 + 0.3 \times 10^{-3} R_B + 0.7$

$12 - 9.99 - 0.7 = 0.3 \times 10^{-3} R_B$

$R_B = \frac{1.31}{0.3 \times 10^{-3}}$

$R_B = 4.3367 \times 10^3 \Omega$

$R_B = 4.3367 K\Omega$

(ii) Stability Factor 'S' :-

$$S = \frac{1+\beta}{1+\beta\left[\frac{R_C}{R_C+R_B}\right]}$$

$$= \frac{1+100}{1+100\left[\frac{330}{330+4.3367}\right]}$$

$$= \frac{101}{1+100\,[0.0708]}$$

$$= \frac{101}{8}$$

$S = 12.5$

Ans :- $R_B = 4.3367 K\Omega$

$S = 12.5$

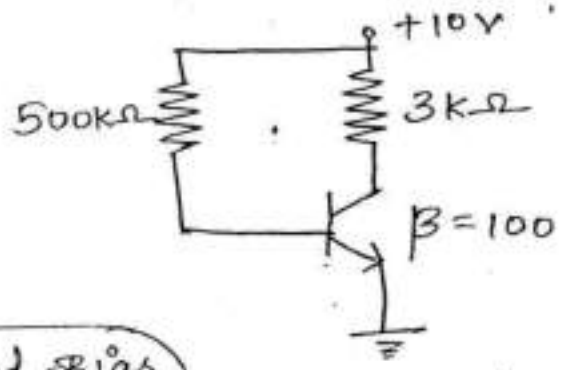
For Good Stabilization S. Value will be low

Collector to Base Bias shows Good Stabilization

S (Fixed Bias) 101 > S (Collector to Base bias) 12.5

---

(20) For the circuit, shown in the figure. Find I_C, V_{CE} and S?.



Hint :- Fixed Bias

Formula :-

i) $I_B = \frac{V_{CC} - V_{BE}}{R_B}$

ii) $I_C = \beta I_B$

iii) $V_{CE} = V_{CC} - I_C R_C$

iv) $S = 1 + \beta$

Given :-

$R_C = 3\,k\Omega = 3 \times 1$

$R_B = 500\,k\Omega = 50$

$\beta = 100$

$V_{CC} = 10V$

$V_{BE} = 0.7V$

Solution :- i) To find I_C :-

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$= \frac{10 - 0.7}{500 \times 10^3}$$

$$= \frac{0.3 \times 10^{-3}}{500}$$

$$I_B = 18.6 \times 10^{-6}$$

$$I_B = 18.6\,\mu A$$

$$I_C = \beta I_B$$

$$= 100 \times 18.6 \times 10^{-6}$$

$$I_C = 1.86 \times 10^{-3}$$

$$I_C = 1.86\,mA$$

ii) Find V_{CE} :-

$$V_{CE} = V_{CC} - I_C R_C$$

$$= 10 - (1.86 \times$$

$$(3 \times 10$$

$$= 10 - 5.58$$

$$V_{CE} = 4.42V$$

iii) $S = 1 + \beta$

$$S = 1 + 100$$

$$S = 101$$

Ans :-

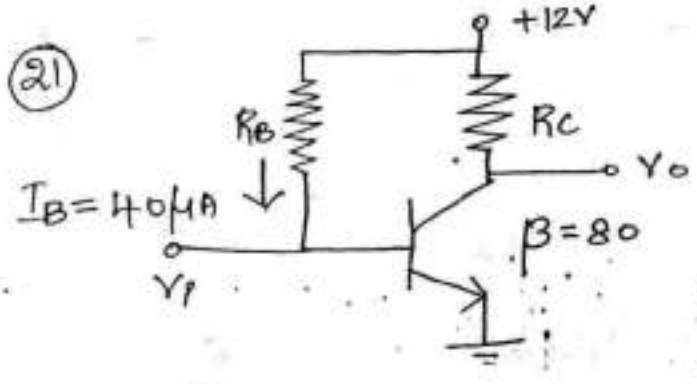
$I_C = 1.86m$

$V_{CE} = 4.42$

$S = 101$

---

(21)



In the circuit given Determine R_B, I_C, R_C.

$V_C = 6V$

Hint:- (fixed Bias circuit)

Formula:- i) $I_B = \frac{V_{cc} - V_{BE}}{R_B}$

ii) $I_C = \beta I_B$

iii) $V_{CE} = V_{cc} - I_C R_C$

Soln:- (i) Find R_B:-

$$V_{cc} - I_B R_B - V_{BE} = 0$$

$$R_B = \frac{V_{cc} - V_{BE}}{I_B}$$

$$R_B = \frac{12 - 0.7}{(40 \times 10^{-6})}$$

$$R_B = \frac{11.3}{40} \times 10^6$$

$$R_B = 0.2825 \times 10^6$$

$$= 282.5 \times 10^{-3} \times 10^6$$

$$R_B = 282.5\ K\Omega$$

(ii) Find I_C:-

$$I_C = \beta \cdot I_B$$

$$= 80 \times 40 \times 10^{-6}$$

$$I_C = 3200 \times 10^{-6}$$

$$= 3.2 \times 10^3 \times 10^{-6}$$

$$= 3.2 \times 10^{-3}$$

$$I_C = 3.2\ mA$$

(iii) Find R_C:-

$$V_{cc} - I_C R_C = V_{CE}$$

$$R_C = \frac{V_{cc} - V_C}{I_C}$$

$$= \frac{12 - 6}{3.2 \times 10^{-3}}$$

$$= \frac{6}{3.2} \times 10^3$$

$$R_C = 1.875\ K\Omega$$

(iv) V_{CE} :-

$$V_{CE} = V_C$$

$$V_{CE} = 6V$$

∴ Ans :-

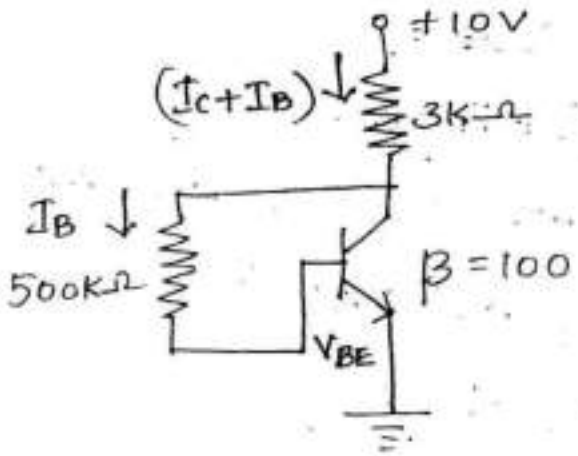
$R_B = 282.5\ K\Omega$

$I_C = 3.2\ mA$

$R_C = 1.875\ K\Omega$

22) For the circuit in Fig Find I_C, V_{CE}, S.

Hint: (Collector to Base Bias)



Given :-

$\beta = 100$

$R_C = 3K\Omega = 3 \times 10$

$R_B = 500K\Omega = 50$

$V_{BE} = 0.7V$

$V_{CC} = 10V$

Formula :-

i) $I_C = \beta \cdot I_B$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_C}$$

ii) $V_{CE} = V_{CC} - (I_B + I_C) R_C$

iii) $$S = \frac{1+\beta}{1+\beta\left[\frac{R_C}{R_C+R_B}\right]}$$

Solo :-

i) Find I_C :-

$$V_{CC} - R_C[I_C + I_B] - I_B R_B - V_{BE} = 0$$

on Simplification,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_C}$$

$$I_B = \frac{10 - 0.7}{500 \times 10^3 + [1+100]\, 3 \times 10^3}$$

$$I_B = 11.58 \times 10^{-6}$$

$$I_B = 11.58 \mu A$$

$$\therefore I_C = \beta \cdot I_B$$

$$= 100 \times 11.58 \times 10^{-6}$$

$$I_C = 1.158 \times 10^{-3}$$

$$\boxed{I_C = 1.158 mA}$$

ii) Find V_{CE} :-

$$V_{CC} - (I_C + I_B) R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - (I_C + I_B) R_C$$

$$= 10 - [11.58 \times 10^{-6} + 1.158 \times 10^{-3}][3 \times 10^3]$$

$$V_{CE} = 10 - [1.169 \times 10^{-3}][3 \times 10^3]$$

$$= 10 - 3.507$$

$$\boxed{V_{CE} = 6.493 V}$$

(iii) S :-

$$S = \frac{1+\beta}{1+\beta\left[\frac{R_C}{R_C + R_B}\right]}$$

$$S = \frac{1+100}{1+100\left[\frac{3 \times 10^3}{3 \times 10^3 + 500 \times 10^3}\right]}$$

$$= \frac{101}{1+100\left[\frac{3 \times 10^3}{503 \times 10^3}\right]}$$

$$= \frac{101}{1+100(0.005964)}$$

$$= \frac{101}{1.5964}$$

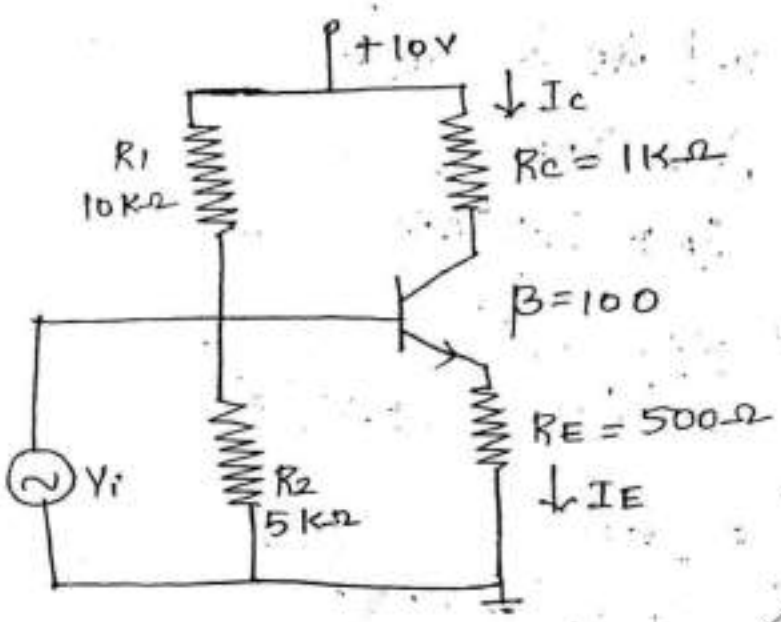
$$\boxed{S = 63.2673}$$

Ans :- $V_{CE} = 6.493V$, $S = 63.2673$, $I_B = 11.58 \mu A$

23) Determine V_{CE} and I_C in the Voltage divider Bias fig is below ..

Hint: Voltage divider Bias

D-07
(8m)



Formula:- i) $V_{CE} = V_{cc} - I_C R_C - I_E R_E$

ii) $I_C = \beta \cdot I_B$

$$I_B = \frac{V_{th} - V_{BE}}{R_B + (1+\beta)R_E} \qquad V_{th} = \frac{R_2}{R_1+R_2} \cdot V_{cc}$$

$$R_B = \frac{R_1 \cdot R_2}{R_1 + R_2}$$

Soln :- i) Find I_C :-

a) V_{th} :- $V_{th} = \frac{R_2}{R_1+R_2} \cdot V_{cc}$

$$= \frac{5\times10^3}{(5\times10^3)+(10\times10^3)} \times 10$$

$$V_{th} = \frac{5\times10^3 \times 10}{15\times10^3}$$

$$V_{th} = \frac{10}{3}$$

$$V_{th} = 3.33V$$

b) R_B :- $R_B = R_1 \,||^{el}\, R_2$

$$R_B = \frac{R_1 R_2}{R_1+R_2} = \frac{(10\times10^3)(5\times10^3)}{(10\times10^3)+(5\times10^3)}$$

$$R_B = \frac{50\times10^6}{15\times10^3}$$

$\therefore R_B = 3.3\times10^3\ \Omega$

Sub V_{th} and R_B in I_B :-

c) $I_B = \dfrac{V_{th} - V_{BE}}{R_B + (1+\beta) R_E}$

$= \dfrac{3.33 - 0.7}{3.3 \times 10^3 + [1+100] \times 500}$

$= \dfrac{2.63}{3.3 \times 10^3 + 50500}$

$I_B = 48.86 \times 10^{-6}$

$I_B = 48.86 \mu A$

d) $I_C = \beta \cdot I_B$

$= 100 \times 48.86 \times 10^{-6}$

$= 4.886 \times 10^{-3}$

$I_C = 4.886 mA$

(ii) Find V_{CE} :-

$V_{CE} = V_{CC} - I_C R_C - I_E R_E \longrightarrow (1)$

$I_E = I_B + I_C$

$= (48.86 \times 10^{-6}) + (4.886 \times 10^{-3})$

$I_E = 4.935 mA$

$\therefore (1) \Rightarrow V_{CE} = 10 - (4.886 \times 10^{-3})(1 \times 10^3) - (4.935 \times 10^{-3})(500)$

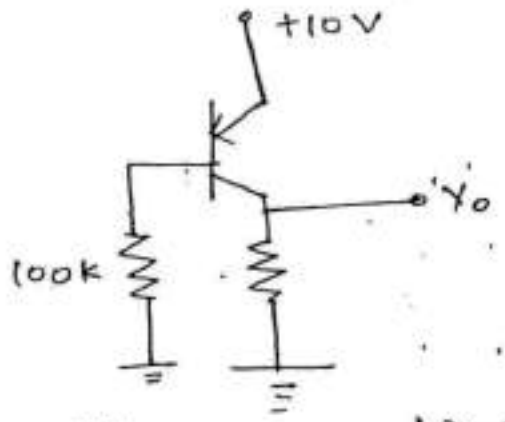
$V_{CE} = 10 - 4.886 - 2.467$

$V_{CE} = 2.647 V$

Ans :- $V_{CE} = 2.647 V$

$I_C = 4.886 mA$

24) The PNP transistor in a circuit of fig. has $\beta = 5$
Find the values of R_C to obtain $V_C = 5V$. What
M-II (8m) happens if the transistor is replaced with Anoth
$\beta = 100$?



Soln:- a) $V_B = V_{CC} - V_{BE}$

$= 10 - 0.7$

$V_B = 9.3V$

b) $I_B = \frac{V_B}{R_B}$

$= \frac{9.3}{100K}$

$I_B = 93\mu A$

i) $\beta = 50$:-

$I_C = \beta I_B$

$= 50 \times 93 \times 10^{-6}$

$I_C = 4.65 \times 10^{-3}$

$I_C = 4.65mA$

$R_C = \frac{V_C}{I_C}$

$= \frac{5}{4.65 \times 10^{-3}}$

$R_C = 1075\Omega$

ii) $\beta = 100$:-

$I_C = \beta I_B$

$= 100 \times 93 \times 10^{-6}$

$I_C = 9.3 \times 10^{-3}$

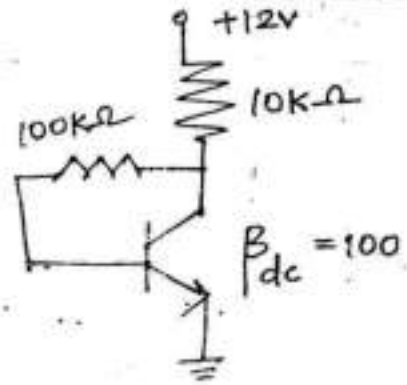
$I_C = 9.3mA$

$R_C = \frac{V_C}{I_C}$

$= \frac{5}{9.3 \times 10^{-3}}$

$R_C = 537.6\Omega$

25)



Calculate the Q point Va
[I_C and V_{CE}] for the circ
in the fig.

Soln:- Hint:- (Collector to Base Bias)

i) To find I_B :-

$$I_B = \frac{V_{cc} - V_{BE}}{R_B + (1+\beta)R_C}$$

$$= \frac{12 - 0.7}{(100 \times 10^3) + (1+100)(10 \times 10^3)}$$

$$I_B = 10.18\mu A$$

(ii) I_C :-

$$I_C = \beta I_B$$

$$= 100 \times 10.18 \times 10^{-6}$$

$$I_C = 1.018 \times 10^{-3}$$

$$I_C = 1.018mA$$

(iii) V_{CE} :-

$$V_{CE} = V_{cc} - (I_B + I_C) R_C$$

$$= 12 - (10.18 \times 10^{-6} + 1.018 \times 10^{-3})(10 \times 10^3)$$

$$V_{CE} = 1.7182V$$

∴ Qpt [1.018mA, 1.7182V]

(26) Calculate the Minimum and Maximum Values of I_C and V_{CE} for the Collector to base bias when $h_{FE}(min) = 50$ and $h_{FE}(max) = 60$. For circuit, $V_{cc} = 12V$, $R_C = 2K$ and $R_B = 150K$. Assume Si transistor. Hint: (Collector to Base Bias)

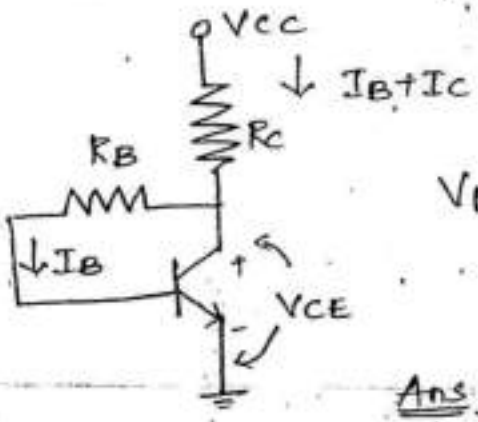
Self:-

:-	$I_B = \frac{V_{cc} - V_{BE}}{(1+\beta)R_C + R_B}$	$I_C = \beta I_B$	$V_{CE} = V_{cc} - I_C R_C - I_B R_C$
min) 50	44.84μA	2.242mA	7.426V
max) 60	41.54μA	2.4924mA	6.932V

(27) Design a collector to Base Bias circuit for the Specified conditions: $V_{CC} = 15V$, $V_{CE} = 5V$, $I_C = 5mA$, $\beta = 100$.

Hint:- Collector to Base Bias

Try by yourself



Formula	Ans.
(i) $I_B = \frac{I_C}{\beta}$	$I_B = 50\mu A$
(ii) $R_C = \frac{V_{CC} - V_{CE}}{I_B + I_C}$	$R_C = 1.98K\Omega$
(iii) $R_B = \frac{V_{CC} - V_{BE}}{I_B}$	$R_B = 86K\Omega$

28) Design a collector to Base Bias circuit to have operating point of (10V, 4mA). The circuit is supplied with 20V and uses a Si transistor of $h_{fe} = 250$.

Given: $\beta = 250$, $V_{CE} = 10V$, $I_C = 4m$, $V_{cc} = 2$

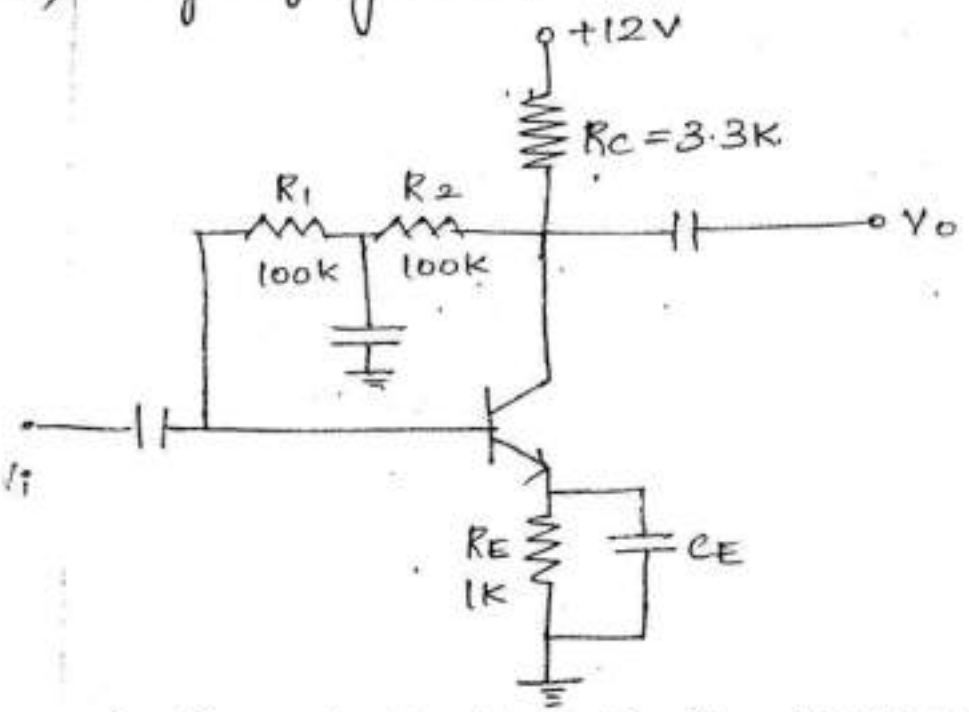
Hint:- Collector to Base Bias

Try by yourself

Formula	Answer
i) $R_C = \frac{V_{CC} - V_{CE}}{I_B + I_C}$	2.49KΩ
ii) $I_B = I_C/\beta$	16μA
iii) $R_B = \frac{V_{CC} - V_{BE}}{I_B}$	581.25KΩ

Draw the circuit diagram.

29) Try by yourself.



Hint: Modified Collector to Base Bias

$R_B = R_1 + R_2$

$R_B = 200K$

for the circuit shown in fig. Determine I_{BQ}, I_{CQ}, V_{CEQ}

Formulas

i) $I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_C + R_E}$

ii) $I_{CQ} = \beta I_{BQ}$

iii) $I_{EQ} = I_{BQ} + I_{CQ}$

iv) $V_{CEQ} = V_{CC} - I_E(R_E + R_C)$

Answers

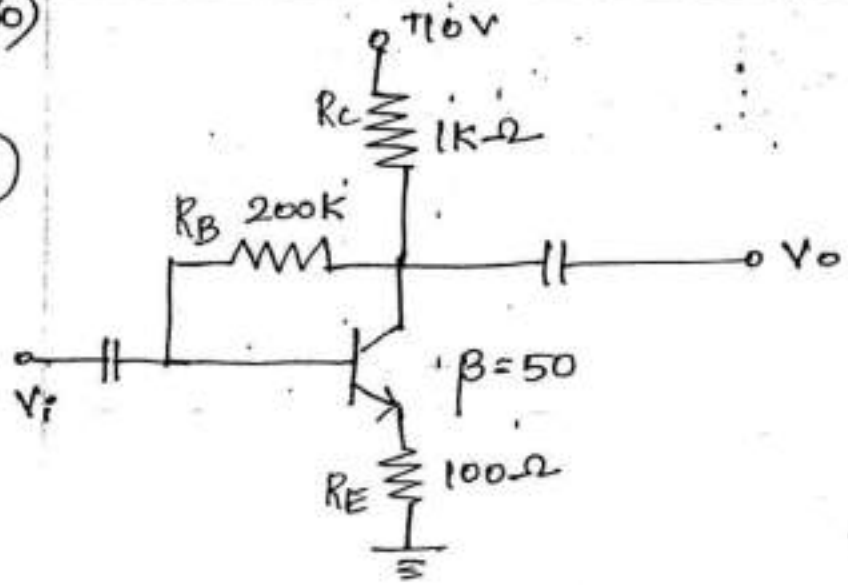
26.95μA

1.347mA

1.3739mA

6.09V

30) M-II (8m)



Hint: Modified Collector to Base Bias

for the circuit shown in the fig. calculate the operating point.

i) Find I_{BQ} :-

$$I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)(R_C + R_E)}$$

$$= \frac{10 - 0.7}{(200 \times 10^3) + (1+50)(1 \times 10^3 + 100)}$$

$$I_{BQ} = 36.31 \mu A$$

ii) Find I_{CQ} :-

$$I_{CQ} = \beta I_{BQ}$$

$$= 50 \times 36.31 \times 10^{-6}$$

$$I_{CQ} = 1.8155 mA$$

iii) Find I_{EQ} :-

$$I_{EQ} = I_{CQ} + I_{BQ}$$

$$= (36.31 \times 10^{-6}) + (1.8155 \times 10^{-3})$$

$$I_{EQ} = 1.85181 mA$$

iv) V_{CEQ} :-

$$V_{CEQ} = V_{CC} - I_E (R_C + R_E)$$

$$= 10 - 1.85181 \times 10^{-3} [1 \times 10^3 + 100]$$

$$V_{CEQ} = 7.963 V$$

∴ Operating point is [1.8155 mA, 7.963 V]

---

3) Determine the Bias Resistor R_B for fixed

Try it Where $V_{CC} = 20V$, $I_B = 2mA$.

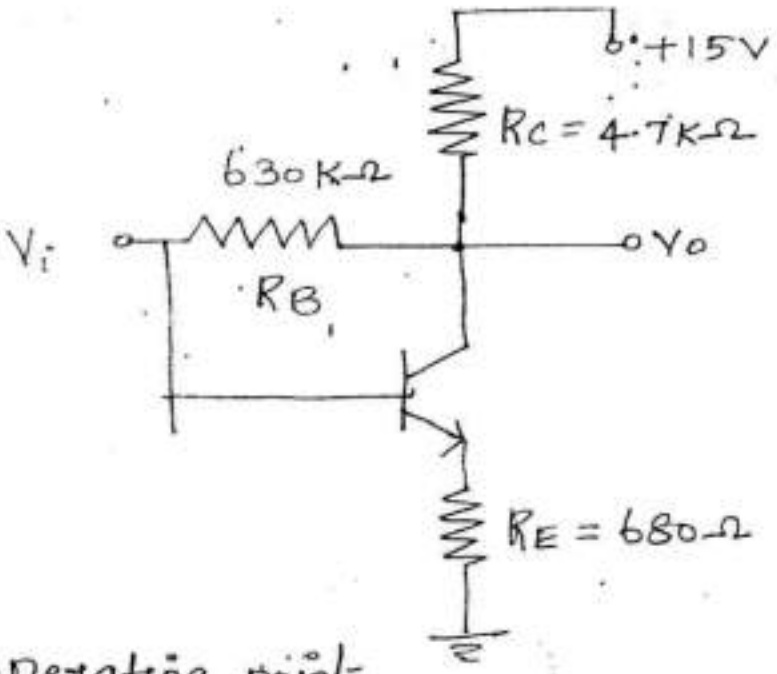
Ans :- $\because R_B = \frac{V_{CC} - V_{BE}}{I_B}$, $\therefore R_B =$

---

32) Locate the operating point of the circuit shown in Fig. $V_{CC} = 15V$, $h_{fe} = 200$.

D-18 (16m)

Hint: (Modified Collector to Base Bias.)



?:- Operating point-

i) I_{BQ} :-

$$I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B + [1+\beta][R_C + R_E]}$$

$$= \frac{15 - 0.7}{630\times10^3 + [1+200][4.7\times10^3 + 680]}$$

$$= 8.356\times10^{-6}$$

$$I_{BQ} = 8.356\,\mu A$$

ii) I_{CQ} :-

$$I_{CQ} = \beta \cdot I_{BQ}$$

$$= 200 \cdot (8.356\times10^{-6})$$

$$I_{CQ} = 1.6712\times10^{-3}$$

$$I_{CQ} = 1.6712\,mA$$

iii) I_{EQ} :-

$$I_{EQ} = I_{CQ} + I_{BQ}$$

$$= (1.6712\times10^{-3}) + (8.356\times10^{-6})$$

$$I_{EQ} = 1.68\times10^{-3}$$

$$I_{EQ} = 1.68\,mA$$

iv) V_{CEQ} :-

$$V_{CEQ} = V_{CC} - I_E[R_C + R_E]$$

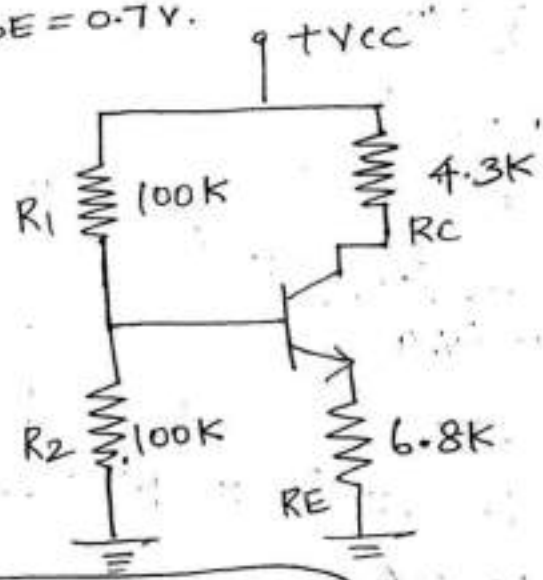
$$= 15 - 1.68 \times 10^{-3}[4.7 \times 10^3 + 680]$$

$$V_{CEQ} = 5.9616V$$

---

33) For the circuit, find the q-point, $V_{CC} = 15V$ and $\beta = 100$, $V_{BE} = 0.7V$.

D-09 (8m)



Hint:- Voltage Divider Bias

Q point $[V_{CE}, I_C]$

i) Find I_C :-

$$I_C = \beta I_B$$

a) $$I_B = \frac{V_{th} - V_{BE}}{R_B + (1+\beta)R_E} \rightarrow (1)$$

b) $$V_{th} = \frac{R_2}{R_1 + R_2} \cdot V_{CC}$$

$$= \frac{100 \times 10^3}{(100 \times 10^3) + (100 \times 10^3)} \times 15$$

$$V_{th} = 7.5V$$

c) $$R_B = R_1 \parallel R_2$$

$$= \frac{R_1 R_2}{R_1 + R_2} \Rightarrow \frac{(100 \times 10^3)(100 \times 10^3)}{(100 \times 10^3) + (100 \times 10^3)}$$

$R_B = 50\,K\Omega$.

Sub V_{th} and R_B in eqn (1) I_B.

$$I_B = \frac{7.5 - 0.7}{(50\times10^3) + (1+100)(6.8\times10^3)}$$

$$I_B = 9.23\times10^{-6}$$

$$I_B = 9.23\,\mu A$$

Sub I_B in I_C.

$$\therefore I_C = \beta \cdot I_B$$

$$= 100 \times 9.23\times10^{-6}$$

$$I_C\beta = 0.923\,mA$$

ii) $$I_E = I_C + I_B$$

$$= (0.923\times10^{-3}) + (9.23\times10^{-6})$$

$$I_E = 0.932\,mA$$

iii) V_{CE} :-

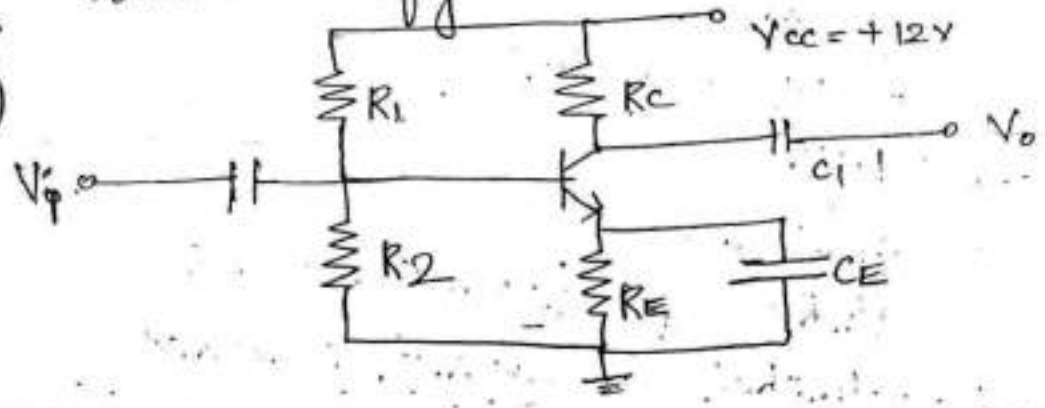
$$V_{CE} = V_{CC} - I_CR_C - I_ER_E$$

$$= 15 - 0.923\times4.3 - 0.932\times6.8$$

$$V_{CE} = 4.6935\,V$$

$\therefore$ operating Q point $[I_{CQ} = 0.932mA;\ V_{CEQ} = 4.6935\,V]$

34) Draw the d.c Load Line for the following transistor Configuration. obtain the Qviescent point



$R_1 = 5.2K$
$R_2 = 1.24\,K$
$R_E = 100\Omega$
$R_C = 330\,\Omega$

Hint :- Voltage Divider Bias

i) Find I_C :-

a) V_{th} :-

$$V_{th} = \frac{R_2}{R_1 + R_2} \cdot V_{cc}$$

$$= \frac{12 \times 1.24 \times 10^3}{(1.24 \times 10^3) + (5.2 \times 10^3)}$$

$$V_{th} = 2.31V$$

b) R_B :-

$$R_B = \frac{R_1 R_2}{R_1 + R_2}$$

$$= \frac{(1.24 \times 10^3)(5}{(1.24 \times 10^3) +}$$

$$(5.2 \times 1$$

$$R_B = 1 \times 10^{-3}$$

$$R_B = 1K\Omega$$

c) I_B :-

$$I_B = \frac{V_{th} - V_{BE}}{R_B + (1+\beta) R_E}$$

$$= \frac{2.31 - 0.7}{(1 \times 10^3) + (1 + 100)(100)}$$

$$= 145 \times 10^{-6}$$

$$I_B = 145\mu A$$

d) I_C :-

$$I_C = \beta \cdot I_B$$

$$= 100 \times 145$$

$$I_C = 14.5 \times 1$$

$$I_C = 14.5mA$$

ii) Find V_{CE} :-

$$V_{CE} = V_{cc} - I_C R_C - I_E R_E$$

$$= 12 - [14.5 \times 10^{-3} \times 330] - [100 \times I_E]$$

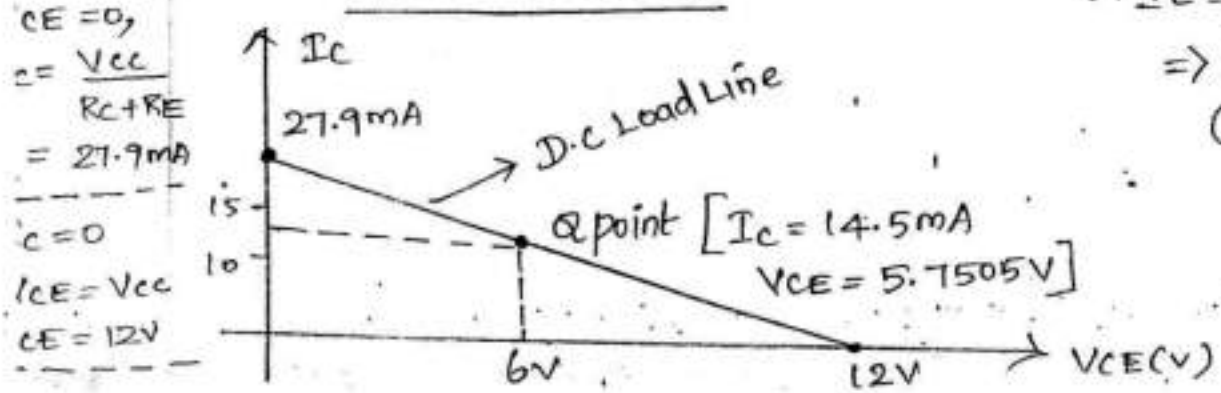
$$= 12 - 4.785 - 100 \times I_E$$

$$V_{CE} = 5.7505V$$

$\therefore I_E = I_B + I$

$\Rightarrow (145 \times 10^{-6}$

$(14.5 \times 10$

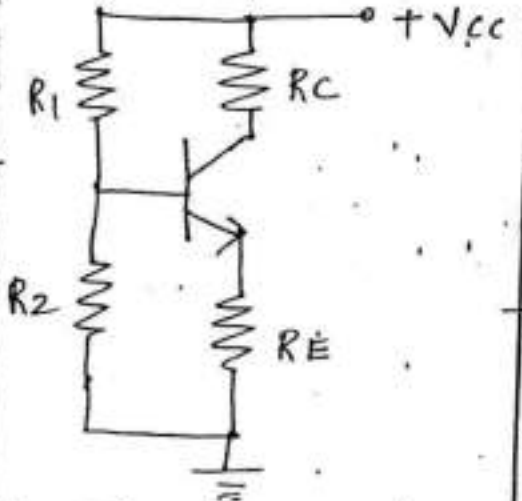


35) Try by yourself.

Calculate the Minimum and Maximum Values of I_C and ~~I_E~~, V_{CE} for the Voltage divider bias, when $h_{FE(min)} = 50$ and $h_{fe(max)} = 60$. for circuit $V_{cc} = 12$, $R_1 = 10K$, $R_2 = 2K$, $R_E = 470\Omega$, $R_C = 2K$. Hint: Voltage divid Bias

Formulas	Answers
	$h_{fe(min)} = 50$
i) $V_{th} = \frac{R_2}{R_1+R_2} \cdot V_{cc}$	$V_{th} = 2V$
ii) $R_B = \frac{R_1 R_2}{R_1+R_2}$	$R_B = 1.67K\Omega$
iii) $I_B = \frac{V_{th} - V_{BE}}{R_B + (1+\beta)R_E}$	$I_B = 50.7\mu A$
iv) $I_C = \beta I_B$	$I_C = 2.535mA$
v) $I_E = I_C + I_B$	$I_E = 2.5857mA$
vi) $V_{CE} = V_{cc} - I_C R_C - I_E R_E$	$V_{CE} = 5.715V$

36) For a circuit shown in fig. $V_{cc} = 20V$, $R_C = 2K\Omega$, $\beta = 50$, $V_{BE} = 0.2V$, $R_1 = 100K\Omega$, $R_E = 100\Omega$. Calculate I_B, V_{CE}, I_C and Stability Factor S.



Hint:- Voltage divider Bias

Formula	Answers
i) $V_{th} = \frac{R_2}{R_1+R_2} \cdot V_{cc}$	1.818V
ii) $R_B = \frac{R_1 R_2}{R_1+R_2}$	9.09KΩ
iii) $I_B = \frac{V_{th} - V_{BE}}{R_B + (1+\beta)R_E}$	114μA
iv) $I_C = \beta I_B$	5.7mA
v) $V_{CE} = V_{cc} - I_C R_C - (1+\beta) I_B R_E$	8V
vi) $S = \frac{1+\beta}{1+\beta[RE/RE+RB]}$	33

4. EMITTER FEEDBACK BIAS (OR) EMITTER STABILIZED BIAS CIRCUIT :

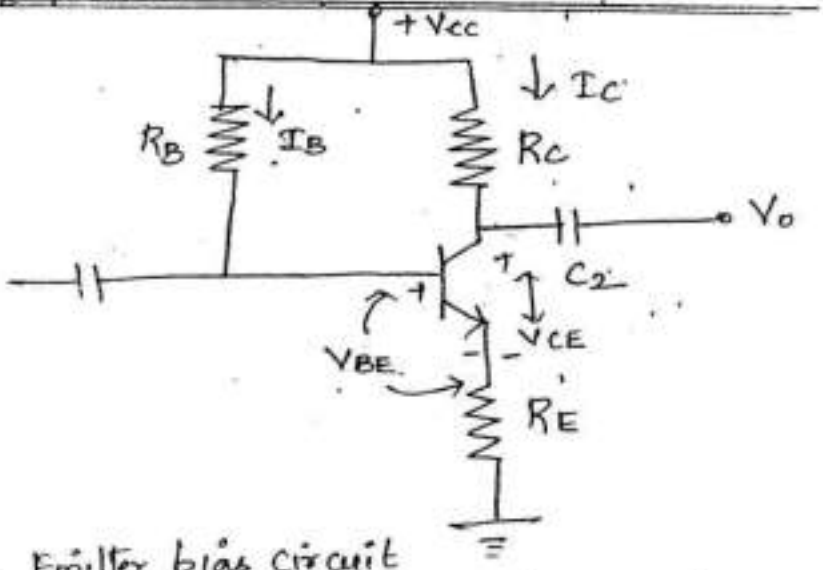
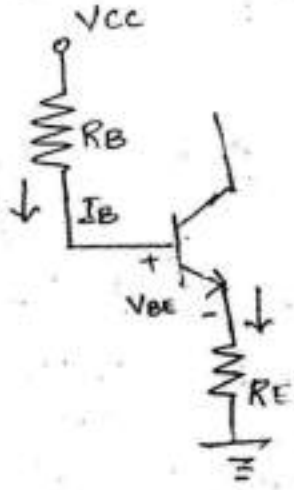


Fig :- Emitter bias circuit

→ To Improve the stability of the biasing circuit over fixed bias stability, the emitter resistance is connected in the biasing circuit. Such biasing circuit is known as emitter bias circuit.

CIRCUIT ANALYSIS:-

(i) BASE CIRCUIT [Input side]



Apply KVL to the base circuit,

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0 \quad \text{—— (1)}$$

$$I_E = I_C + I_B \quad \text{—— (2)}$$

$$= I_B + \beta I_B$$

$$I_E = (\beta + 1) I_B \quad \text{—— (3)}$$

Sub (3) in (1)

$$V_{CC} - I_B R_B - V_{BE} - (1+\beta) I_B R_E = 0$$

$$V_{CC} - V_{BE} = I_B R_B + (1+\beta) I_B R_E$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_E}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta R_E} \quad (\because \beta >> 1)$$

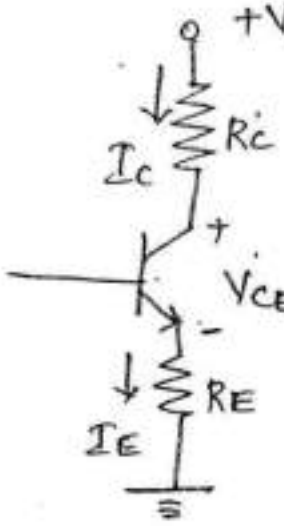
only difference is βR_E with fixed Bias.

$$V_B = V_{BE} + V_E$$

$$V_E = I_E R_E$$

$$V_B = V_{BE} + I_E R_E$$

(ii) Collector circuit (output side) :-



Apply KVL to the collector circuit

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$V_{CE} = V_C - V_E$$

$$V_C = V_{CC} - I_C R_C$$

Qun :- (i) Draw and explain emitter feedback Bias. (8m) [M-14, D-12]

PROBLEMS CONTINUATION :-

37) For a Voltage divider Bias, $V_{CC} = 5V$, $\beta = 100$ and $R_C = 1.2K\Omega$. obtain the values of R_E, R_1 and R_2 such that the circuit is considered bias stable at $V_{CEQ} = 3V$.

Hint :- Voltage divider Bias

Given :- $V_{CC} = 5V$, $R_C = 1.2K\Omega$, $R_E, R_1, R_2 = ?$, $\beta = 100$, $V_{CEQ} = 3V$

Soln :- i) I_{CQ} :-

$$I_{CQ} = \frac{V_{CC} - V_{CEQ}}{R_C + R_E}$$

$$= \frac{5-3}{1.2 + 0.68}$$

$$I_{CQ} = 1.064\ mA$$

ii) R_E :-

$$R_E = I_{CQ} \times R_E \Rightarrow 1.064 \times 10^{-3} \times 0.68 \times 10^{3}$$

$R_E = 0.7235V$

(iii) I_B :-

$$I_{BQ} = \frac{I_{CQ}}{\beta}$$

$$= \frac{1.064 \times 10^{-3}}{100}$$

$$I_{BQ} = 10.64\,\mu A$$

(iv) R_B (or) R_{th} :-

$$I_{BQ} = \frac{V_{th} - V_{BE}}{R_B + (1+\beta)R_E}$$

for bias stable, $R_B = 0.1(1+\beta)R_E$

$$R_B = 0.1[1+100] \times 680$$

$$R_B = 6.868\,K\Omega$$

(v) V_{th} :-

$$I_{BQ} = \frac{V_{th} - V_{BE}}{R_B + (1+\beta)R_E}$$

$$V_{th} = I_{BQ}[R_B + (1+\beta)R_E] + V_{BE}$$

$$= 10.64 \times 10^{-6}[6.868 \times 10^3 + (1+100) \times 680] + 0.7$$

$$V_{th} = 1.5V$$

(vi) R_1 and R_2 :-

$$V_{th} = \frac{R_2}{R_1 + R_2} \cdot V_{CC}$$

$$\frac{R_2}{R_1+R_2} = \frac{V_{th}}{V_{CC}} \Rightarrow \frac{1.5}{5} \Rightarrow 0.3$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2} \Rightarrow R_1\left[\frac{R_2}{R_1+R_2}\right] \Rightarrow 0.3R_1$$

$$R_1 = \frac{R_B}{0.3} = \frac{6.868K}{0.3}$$

$$R_1 = 22.86K\Omega$$

$$R_2 = \frac{1}{1/R_B - 1/R_1} \Rightarrow \frac{1}{6.868 \times 10^3 - 1/22.86 \times 10^3}$$

Try by yourself

Design a Voltage divider Bias circuit for the specified Conditions. $V_{CC} = 12V$, $V_{CE} = 6V$, $I_C = 1mA$, $S = 20$, $\beta = 100$, $V_E = 1V$.

Voltage divider Bias

i) $I_B = \frac{I_C}{\beta} \Rightarrow 10\mu A$

ii) $I_E = I_B + I_C = 1.01mA$

iii) $R_E = \frac{V_E}{I_E} = 990\Omega$

iv) $R_C = \frac{V_{CC} - V_{CE} - V_E}{I_C} = 5K\Omega$

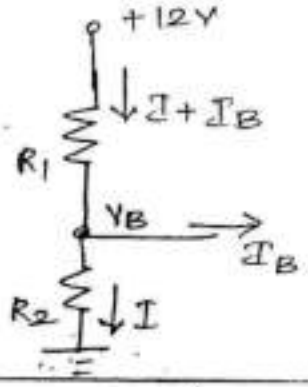
v) $S = \frac{1+\beta}{1+\beta\left[\frac{R_E}{R_B+R_E}\right]}$, $R_B = 23454\Omega$

vi) $V_B = V_E + V_{BE} = 1.7V$

vii) $R_1 = \frac{V_{CC} - V_B}{I + I_B} \Rightarrow R_1 = 145.486\Omega$

viii) $R_2 = \frac{1.7}{I} \Rightarrow R_2 = 27961.9\Omega$

$[I = 60.797\mu A]$

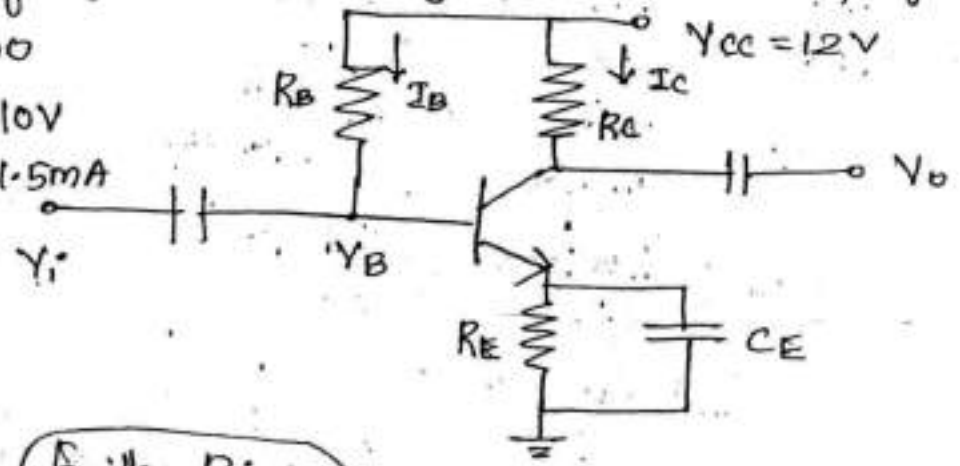


39) Determine the resistor values of the circuit shown in fig. for given operating point and supply voltage.

$\beta = 100$

$V_{CEQ} = 10V$

$I_{CQ} = 1.5mA$



Hint: Emitter Bias

Let us Assume $V_E = \frac{1}{10}$ of V_{cc}.

i) $V_E = \frac{1}{10}(20) \Rightarrow V_E = 2V$

ii) I_{BQ} :- $I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{1.5\times10^{-3}}{100}$

$$I_{BQ} = 15\mu A$$

(iii) $R_E = \frac{V_E}{I_E} = \frac{V_E}{I_B + I_C} = \frac{2}{(15\times10^{-6}) + (1.5\times10^{-3})}$

$$R_E = 1.32K\Omega$$

iv) $R_C = \frac{V_{cc} - V_{CE} - V_E}{I_C}$

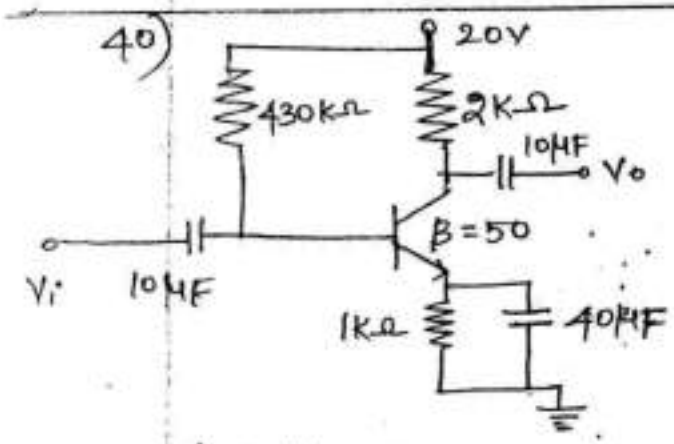
$$= \frac{20-10-2}{1.5\times10^{-3}} \Rightarrow R_C = 5.33K\Omega$$

v) $R_B = \frac{V_{cc} - V_{BE} - V_E}{I_B} \Rightarrow \frac{20-0.7-2}{15\times10^{-6}}$

$$R_B = 1.15M\Omega$$

---

40)



for the Emitter Bias Network. Determine I_B, I_C, V_{CE}, V_C, V_E, V_B and V_{BC}.

Soln:- Hint:- Emitter Bias ckt

Ans:- i) $I_B = \frac{V_{cc} - V_{BE}}{R_B + (1+\beta)R_E} = 40.125\mu A$

ii) $I_C = \beta I_B = 2.00625mA$

iii) $I_E = I_B + I_C = 2.046875mA$

Try by yourself

(iv) $V_{CE} = V_{cc} - I_C R_C - I_E R_E$

$V_{CE} = 13.94V$

(v) $V_C = V_{cc} - I_C R_C$

$V_C = 15.9875V$

(vi) $V_E = I_E R_E = 2.0468$

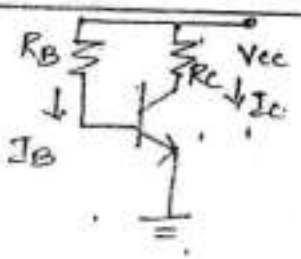
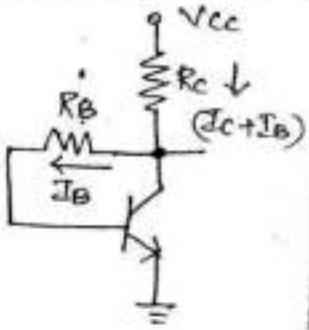
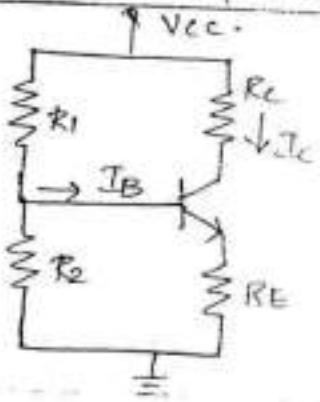
(vii) $V_B = V_E + V_{BE}$

$V_B = 2.746375$

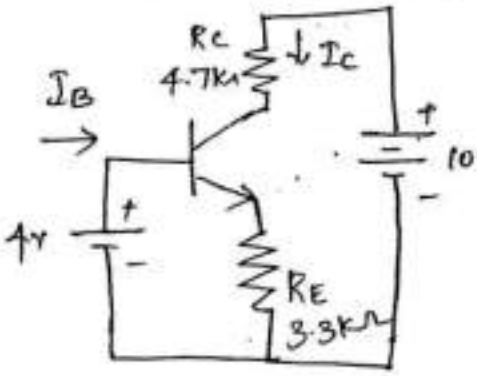
(viii) $V_{BC} = V_B - V_C$

$V_{BC} = -13.24$ V

Comparison of Biasing Circuits - Comment. Qun.

Biasing Circuits	Fixed Bias	Collector to Base Bias	Voltage Divider Bias
Circuit			
Stability	Less	Medium	Highest
Feedback	No	Voltage Shunt Negative feedback	current Series Negative feedback
Application	Used in Circuits Where Stability is not important criteria	It is used in Switching circuits	It is most perfered biasing circuit the transistor from going into Saturation. It is used in circuits Where Stability Requirements are Needed
$V_{CE(min)}$	3V	6.932V	5.632V
$V_{CE(max)}$	4.466V	7.426V	5.715V

- **Problems Continuation:-**

41) 

by yourself

for the circuit shown in the fig. $\beta = 100$. Calculate V_E, I_E, I_C and V_C.

Ans:-

i) $V_E = V_B - V_{BE} = 3.3V$

ii) $I_E = \frac{V_E}{R_E} = 1mA$

iii) $I_E = I_C + I_B$, $I_B = \frac{I_E}{1+\beta}$

$I_E = 0.99mA$

iv) $V_C = V_{CE} - I_C R_C \Rightarrow 5.347V$

Biasing :- In JFET, drain current I_D changes with temp. Hence Q-point changes. In order to obtain the stable Q-point JFET is biased for zero temp drift. The Q-point is selected in the Middle of the transfer characteristics (or) drain characteristics.

(2m)

(*) FET Biasing :- MOSFET

(2m)

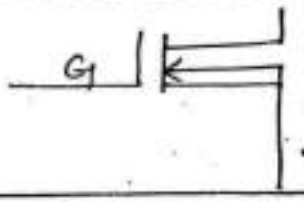
→ The Similarities in Appearance between the transfer curves of JFET and depletion-type MOSFET permit a similar Analysis in the d.c. domain.

→ The primary difference between the two is the fact that depletion-type MOSFET permit operating points with positive values of V_{GS} and levels of I_D that exceeds I_{DSS}.

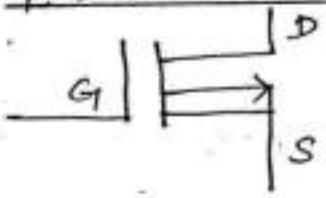
→ The Analysis is the same if the JFET is Replaced by a depletion-type MOSFET.

→ The procedure followed for Analysis of DMOSFET biasing circuits is exactly same as the one followed for the JFET biasing circuits.

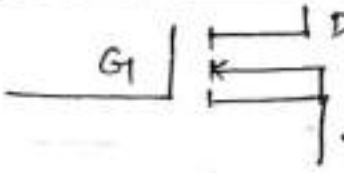
(i) N-channel D-MOSFET



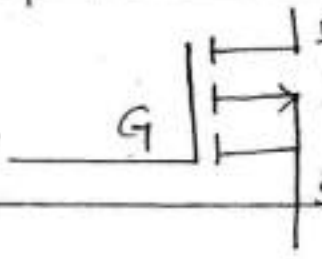
(ii) P-channel D-MOSFET



(iii) N-channel E-MOSFET



(iv) P-channel E-MOSFET



D - Depletion type.

E - Enhancement type.

$$I_D = K\left[V_{GS} - V_{GS(Th)}\right]^2$$

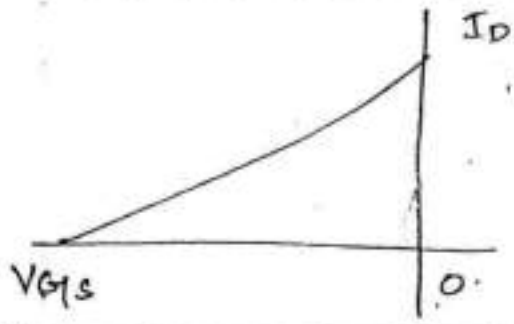
$$K = I_{D(ON)} / \left[V_{GS(ON)} - V_{GS(Th)}\right]^2$$

→ V_{GS} Must be greater than V_{Th}, $V_{GS} > V_{Th}$

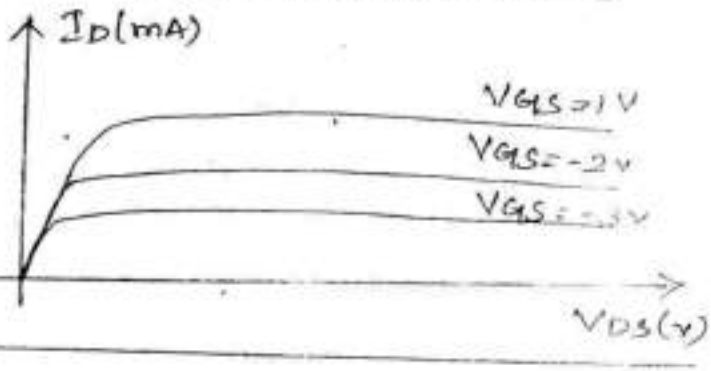
→ Threshold Voltage Must be 2V

i) D-MOSFET

Transfer characteristics

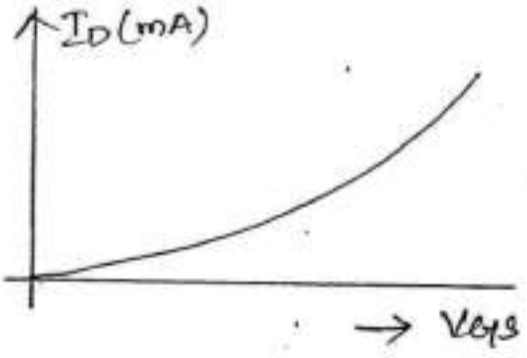


Drain characteristics

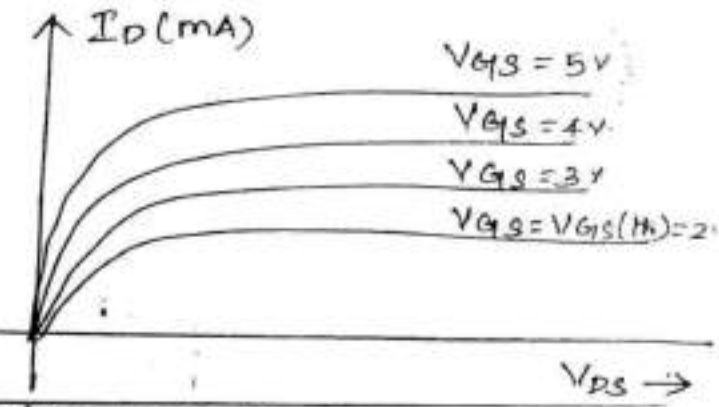


ii) E-MOSFET

Transfer characteristics



Drain characteristics



IC 6: DESIGN OF BIASING FOR MOSFET

i) D-MOSFET Biasing

1. Gate Bias [Fixed Bias]
2. Self Bias
3. Voltage divider Bias

ii) E-MOSFET Biasing

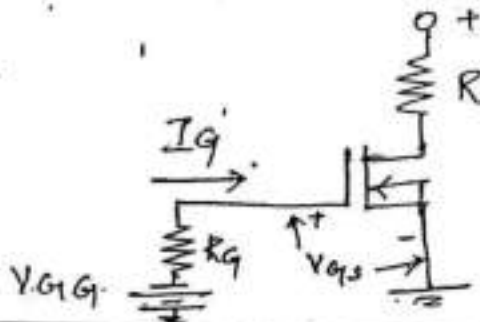
1. Voltage divider Bias
2. Drain Feedback Bias

i) D-MOSFET Biasing :-

1. Fixed Bias / Gate Bias Method :-

(X) [Same derivation as JFET fixed Bias]

Fig :-

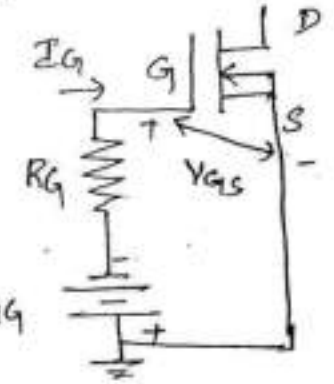


for d.c. Analysis,

$I_G = 0$

$I_D = I_S$ (X)

(i) Input circuit:- [Gate side].



Apply KVL at the Gate s:

$-V_{GG} - I_G R_G - V_{GS} = 0$

$I_G = 0$

$-V_{GG} - 0 - V_{GS} = 0$

$\boxed{-V_{GG} = V_{GS}}$

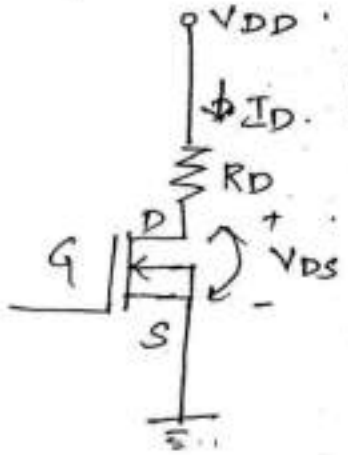
(ii) Shockley's eqn:-

$$\boxed{I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2}$$

$V_{GS} = -V_{GG}$

$$I_D = I_{DSS}\left[1 + \frac{V_{GG}}{V_P}\right]^2$$

(iii) output circuit [Drain side]



Apply KVL at Drain side,

$V_{DD} - I_D R_S - V_{DS} = 0$

$\boxed{V_{DS} = V_{DD} - I_D R_S}$

$\therefore V_{DS} = V_D - V_S$

$V_{GS} = V_G - V_S$

$\therefore V_S = 0$

$V_{DS} = V_D, \quad V_{GS} = V_G$.

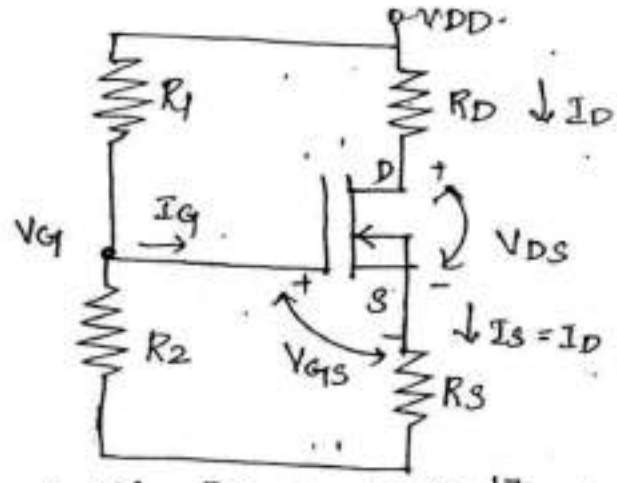
---

2. Voltage divider Bias Method:-

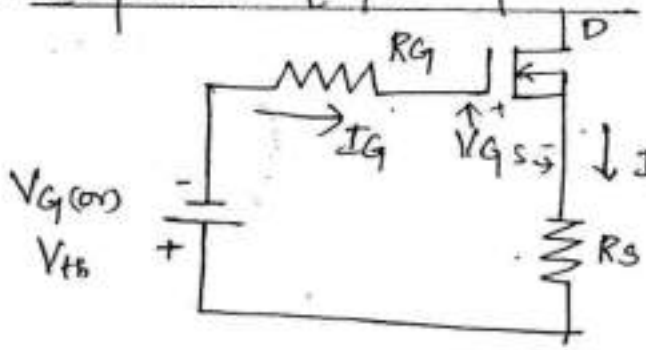
→ The N-channel JFET like N-channel D-MOSFET is given by,

(X) [Same derivation as JFET Voltage divider Bias

Fig:-



(i) Input Side [Gate Method]



Apply KVL at input

$V_G - R_G I_G - V_{GS} - I_S R_S = 0$

$[\because I_G = 0]$

$V_G - V_{GS} - I_D R_S = 0$

$[\because I_D = I_S]$

$$\boxed{V_{GS} = V_G - I_D R_S}$$

(ii) V_G :-

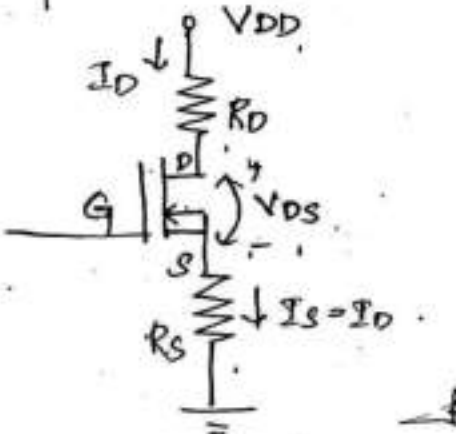
$$V_G = \frac{R_2}{R_1 + R_2} \times V_{DD}$$

(iii) Shockley's equation.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$I_D = I_{DSS}\left[1 - \frac{(V_G - I_D R_S)}{V_P}\right]^2$$

(iv) Output Side [Drain Side].



Apply KVL at output,

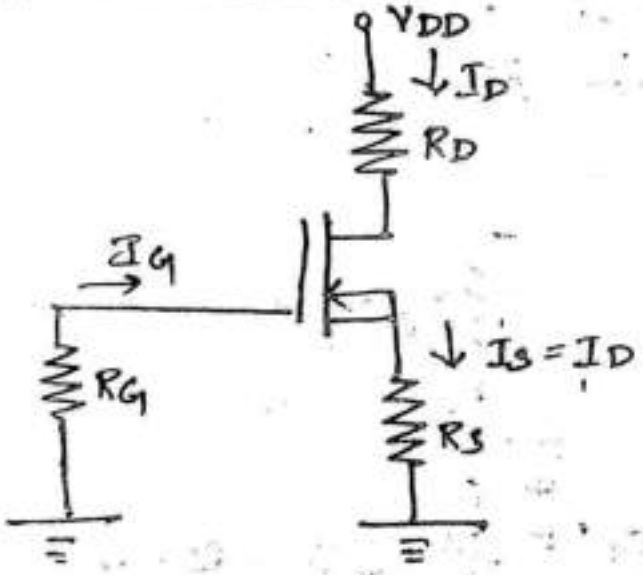
$V_{DD} - I_D R_D - V_{DS} - I_S R_S = 0$

$V_{DD} - I_D R_D - V_{DS} - I_D R_D = 0$

$$\boxed{V_{DS} = V_{DD} - I_D[R_D + R_S]}$$

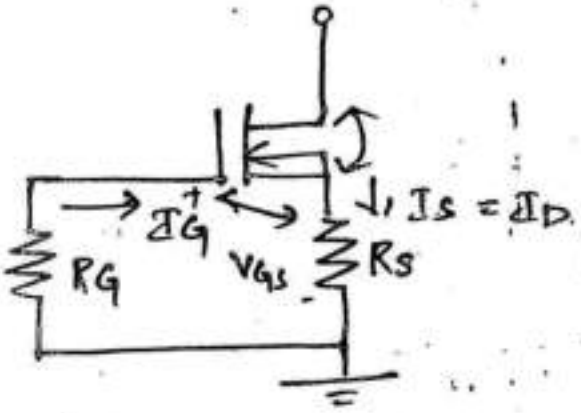
The Q-point of D-MOSFET are I_D, V_{DS}, V_{GS}.

3. SELF BIAS METHOD:-



This is most common type Biasing.

(i) Input Side:- [Gate]



Apply KVL at input (Gate).

$-I_G R_G - V_{GS} - I_S R_S = 0$

$0 - V_{GS} - I_S R_S = 0$

$(I_G = 0)$

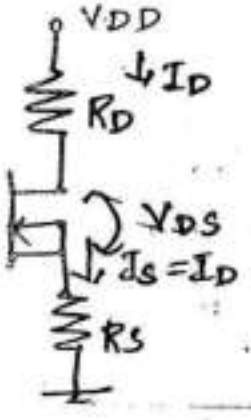
$$\boxed{V_{GS} = -I_S R_S}$$

(ii) Shockley's equation:

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$I_D = I_{DSS}\left[1 + \frac{I_D R_S}{V_P}\right]^2$$

(iii) output Side:-



Apply KVL at output

$V_{DD} - I_D R_D - V_{DS} - I_S R_S = 0$

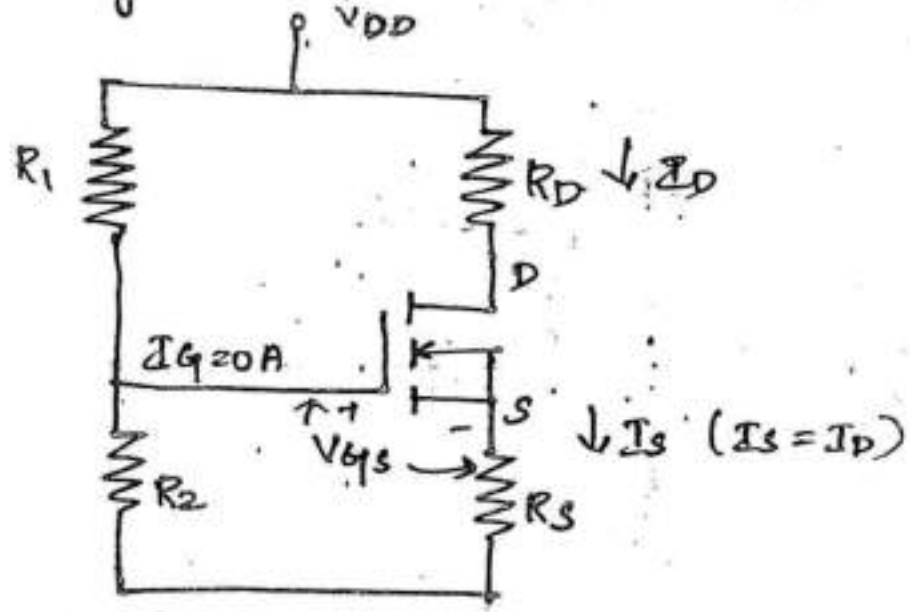
$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$

$$\boxed{V_{DS} = V_{DD} - I_D(R_D + R_S)}$$

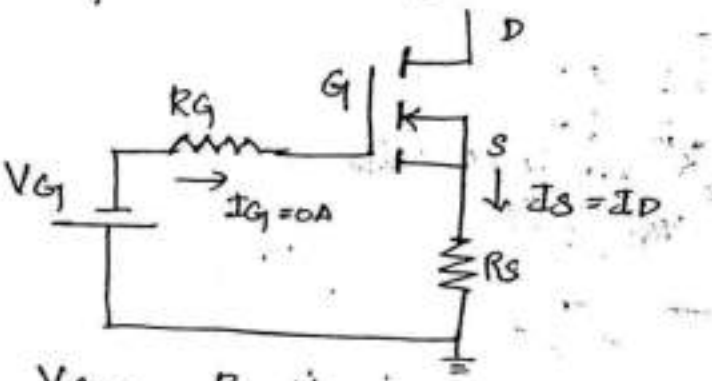
(ii) E-MOSFET BIASING:-

1. Voltage divider Bias:-

fig:-



(i) Input side [Gate circuit] :-



Apply KVL at Gate side,

$V_G - R_G I_G - V_{GS} - I_S R_S = 0$

$[I_G = 0,\ I_S = I_D]$

$V_G - 0 - V_{GS} - I_D R_S = 0$

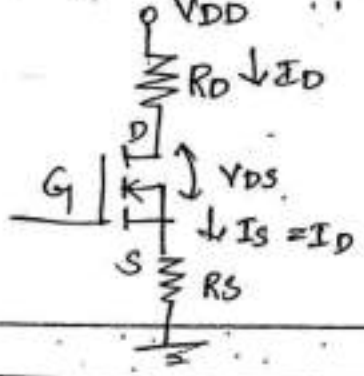
$V_{GS} = V_G - I_D R_S$

(ii) $V_G = \dfrac{R_2 \cdot V_{DD}}{R_1 + R_2}$

(iii) Shockley's equation, $I_D = K[V_{GS} - V_{GS(Th)}]^2$

$K = \dfrac{I_{D(ON)}}{[V_{GS(ON)} - V_{GS(TH)}]^2}$

(iv) output side [Drain circuit]



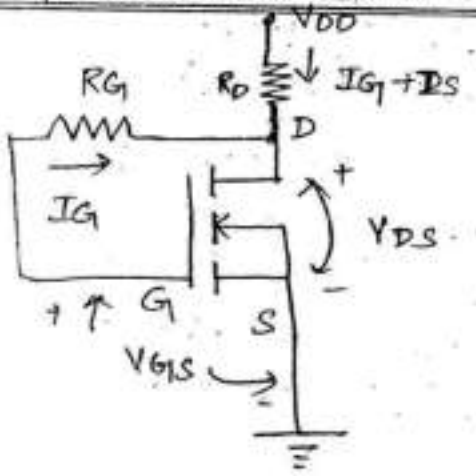
Apply KVL at output side,

$V_{DD} - I_D R_D - V_{DS} - I_S R_S = 0$

$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$

$V_{DS} = V_{DD} - I_D[R_D + R_S]$

2. **DRAIN FEEDBACK BIAS CIRCUIT:-**



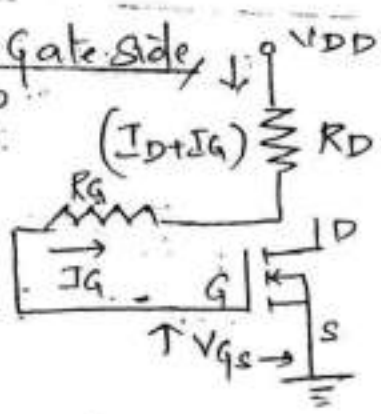
A popular Biasing Arrangement for E-ty MOSFET.

$\therefore I_G = 0$

$V_{RG} = 0$

(i) Input side [Gate side]

Apply KVL at Gate side,



$$V_{DD} - (I_D + I_G) R_D - I_G R_G - V_{GS} = 0$$

$(I_G = 0)$

$$V_{DD} - I_D R_D - I_G R_D - I_G R_G - V_{GS} = 0$$

$$V_{DD} - I_D R_D - I_G R_G - V_{GS} = 0$$

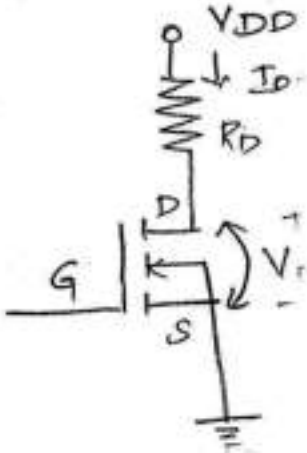
$$\boxed{V_{DD} - I_D R_D = V_{GS}}$$

(ii) Shockley's eqn, $\boxed{I_D = K\left[V_{GS} - V_{GS(TH)}\right]^2}$

$$K = \frac{I_{D(ON)}}{\left[V_{GS(ON)} - V_{GS(TH)}\right]^2}$$

(iii) output Side [Drain side]

Apply KVL at o/p side,



$$V_{DD} - (I_D + I_G)(R_D) - V_{DS} = 0$$

$$V_{DD} - R_D I_D - R_D I_G - V_{DS} = 0$$

$(\because I_G = 0)$

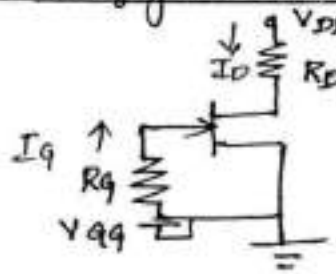
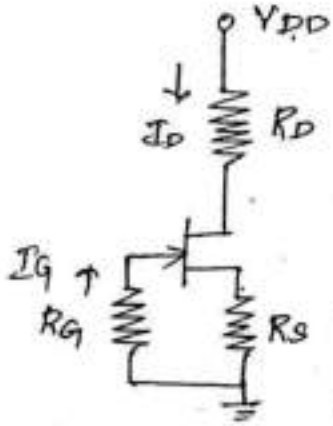
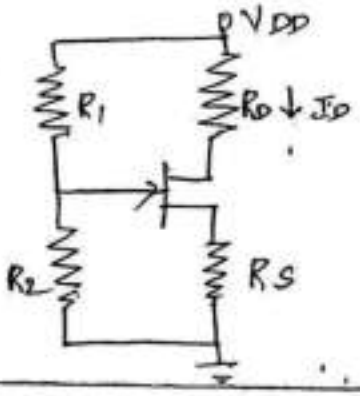
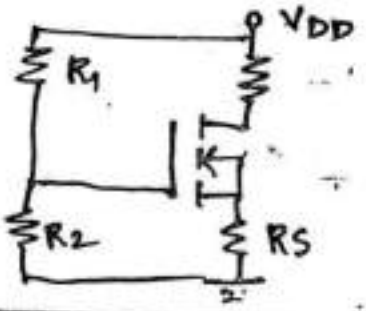
$$V_{DD} - R_D I_D - 0 - V_{DS} = 0$$

$$V_{DD} - R_D I_D = V_{DS}$$

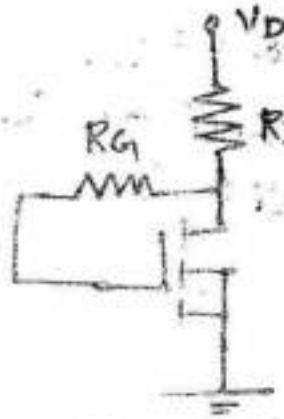
$$\boxed{V_{DS} = V_{DD} - R_D I_D}$$

(*) Explain E-MOSFET Biasing Methods.
(*) Explain D-MOSFET Biasing Methods.
(*) Explain D-MOSFET Voltage divider Bias.
(*) Explain Self Bias of D-MOSFET and E-MOSFET
(*) Explain Gate Bias (fixed Bias) of E-MOSFET and D-MOSFET
(*) Explain E-MOSFET drain feedback Bias.
(*) Explain E-MOSFET Voltage divider Bias.
[M-15, M-16, A-15, A-14, N-13, N-10, M-9]

Ans:- [Above]

Type- Configuration.	V_{GS}	V_{DS}
JFET fixed Bias 	$V_{GS} = -V_{GG}$	$V_{DS} = V_{DD} - I_D R_S$
JFET self Bias 	$V_{GS} = -I_D R_S$	$V_{DS} = V_{DD} - I_D (R_D + R_S)$
JFET voltage divider Bias 	$V_G = \frac{R_2}{R_1+R_2} \cdot V_{DD}$ $V_{GS} = V_G - I_D R_S$	$V_{DS} = V_{DD} - I_D [R_D + R_S]$
D-MOSFET voltage divider Bias 	$V_G = \frac{R_2}{R_1+R_2} \cdot V_{DD}$ $V_{GS} = V_G - I_D R_S$	$V_{DS} = V_{DD} - I_D (R_D + R_S)$

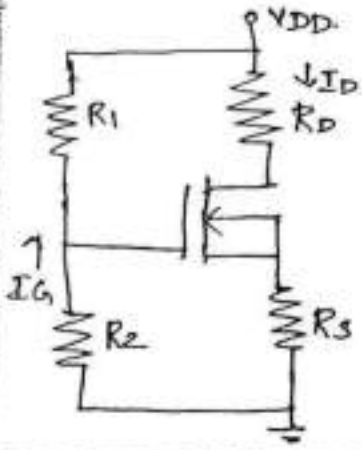
E-MOSFET Drain feedback bias



$V_{GS} = V_{DS}$

$V_{GS} = V_{DD} - I_D R_D$

-MOSFET Voltage divider Bias

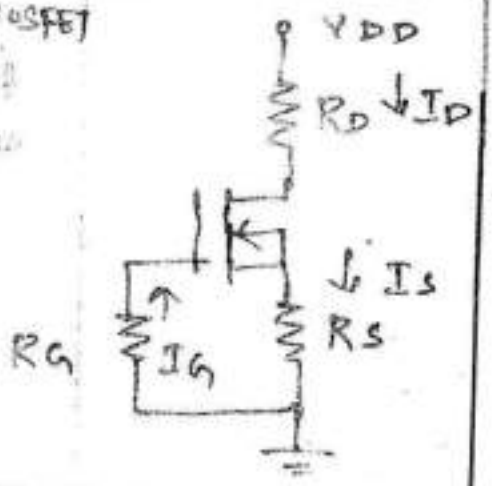


$V_G = \frac{R_2}{R_1+R_2} \cdot V_{DD}$

$V_{GS} = V_G - I_D R_S$

$V_{DS} = V_{DD} - I_D(R_D + R_S$

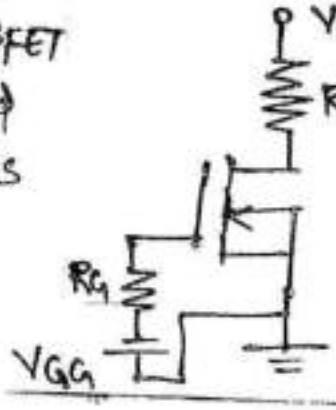
-MOSFET Self Bias



$V_{GS} = -I_D R_S$

$V_{DS} = V_{DD} - I_D [R_D +$

MOSFET fixed bias



$V_{GS} = -V_{GG}$

$V_{DS} = V_{DD} - I_D R_S$

-MOSFET - Drain feedback Bias, Voltage divider Bias.

$I_D = K[V_{GS} - V_{GS(TH)}]$, $K = \frac{I_{D(ON)}}{[V_{GS(ON)} - V_{GS(TH}]}$

remaining:- $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$

64) Problems Continuation:- [JFET / MOSFET]. (11)

Calculate the Value of feedback Resistor (R_S) required to Self Bias an N-Channel JFET with $I_{DSS} = 40mA$ $V_P = -10V$ and $V_{GSQ} = -5V$.

Soln:- Hint: [Self Bias - JFET]

(i) I_D:-

a) $V_{GS} = -I_D R_S$.

b) $R_S = \left|\frac{V_{GS}}{I_D}\right| = \frac{-5}{I_D}$. $\longrightarrow$ (1)

c) $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$

$= 40\times10^{-3}\left[1 - \frac{(-5)}{-10}\right]^2$

$= 40\times10^{-3}\left[1 - 0.5\right]^2$

$= 40\times10^{-3}\left[0.5\right]^2$

$I_D = 10\times10^{-3}$

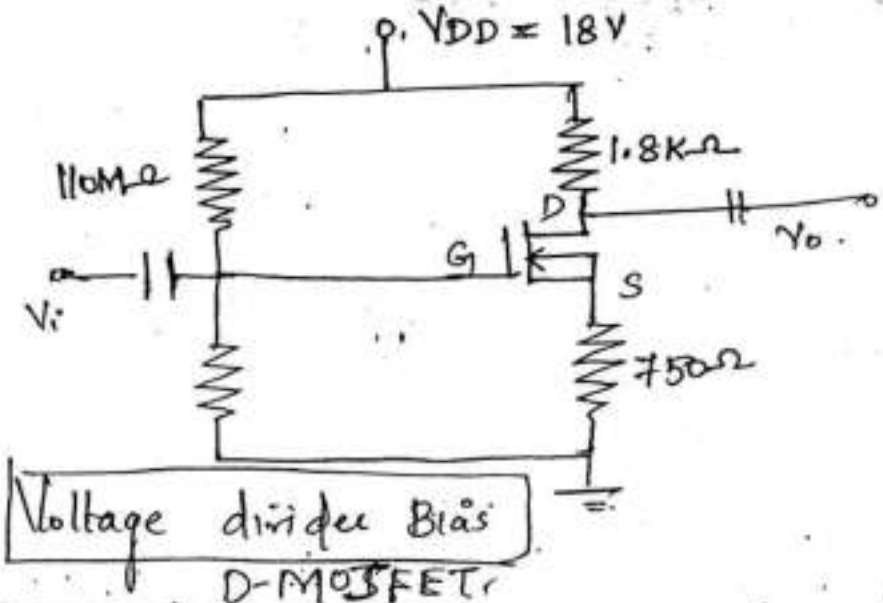
$I_D = 10mA$. $\longrightarrow$ (2)

Sub (2) in (1).

$R_S = \left|\frac{-5}{10\times10^{-3}}\right| \Rightarrow \underline{R_S = 500\Omega}$.

---

65) For the circuit, shown in Fig. calculate I_{DQ} and V_{DSQ}



Hint:- [Voltage divider Bias] D-MOSFET.

Soln :-

(i) V_G :- $V_G = \frac{R_2}{R_1 + R_2} \times V_{DD}$

$= \frac{10 \times 10^6 \times 18}{(10+110) \times 10^6}$

$V_G = 1.5V$

(ii) I_D :- $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$

$= 6 \times 10^{-3}\left[1 - \frac{(1.5 - 750 I_D)}{V_P}\right]^2$

$= 6 \times 10^{-3}\left[1 + 0.5 - 250 I_D\right]^2$

$= 6 \times 10^{-3}\left[1.5 - 250 I_D\right]^2$

$= 6 \times 10^{-3}\left[2.25 - 750 I_D + 62500 I_D^2\right]$

$I_D = 0.0135 - 4.5 I_D + 375 I_D^2$

$375 I_D^2 - 5.5 I_D + 0.0135 = 0$

$I_D = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$

$= \frac{-5.5 \pm \sqrt{(-5.5)^2 - 4(375 \times 0.0135)}}{2 \times 375}$

$I_D = 11.55mA$ (or) $3.11mA$

a) V_{GS} :-

$V_{GS} = V_G - I_D R_S$

$V_{GS} = 1.5 - 750 I_D$

$V_P = -3V$

$I_D = 11.55mA$

(iii) $V_{DS} = V_{DD} - I_D(R_D + R_S)$

$= 18 - 11.55 \times 10^{-3}[1.8 + 0.75] \times 10^3$

$= -11.45V$

V_{DS} is practically Not Acceptable. choose.

$I_D = 3.11mA$

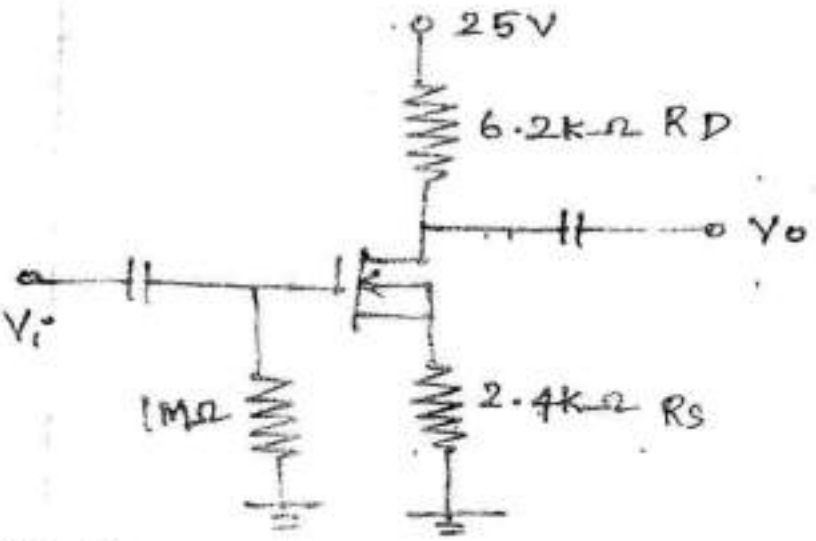
$V_{DS} = V_{DD} - I_D(R_D + R_S)$

$= 18 - 3.11 \times 10^{-3}[1.8 + 0.75] \times 10^3$

$V_{DS} = 10.07V$

66) Determine following for given circuit (i) I_{DQ} (ii) V_{GSQ} (iii) V_{DS}. (12)

Hint: D-MOSFET Self Bias



$I_{DSS} = 8mA$

$V_p = -8V$

Solo:- i) V_{GS} :- $V_{GS} = -I_D R_S = -2.4 I_D \longrightarrow (1)$

ii) I_D :- $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2$

$= 8 \times 10^{-3}\left[1 - \frac{(-2.4 I_D)}{-8}\right]^2$

$\Rightarrow 8 I_D = 64 - 38.4 I_D + 5.76 I_D^2$

$5.76 I_D^2 - 46.4 I_D + 64 = 0$

$\therefore I_D = \frac{46.4 \pm \sqrt{(46.4)^2 - 4 \times 5.76 \times 64}}{2 \times 5.76}$

$I_D = 6.29mA$ (or) $1.77mA$

$I_D = 6.29mA$, $V_{DS} \rightarrow$ Negative.

Choose $I_D = 1.77mA$

$V_{GSQ} = -2.4 I_D$

$= -2.4 \times 1.77 \times 10^{-3}$

$V_{GSQ} = -4.24V.$

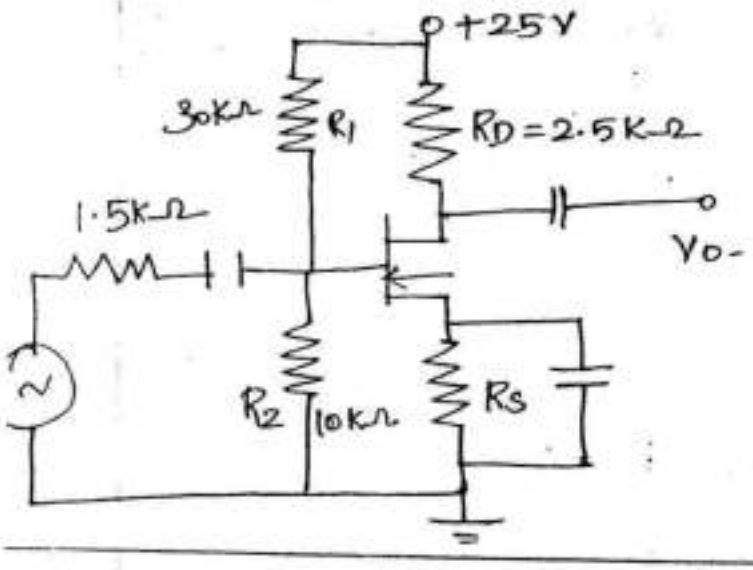
iii) V_{DS} :- $V_{DS} = V_{DD} - I_D R_D$

$= 20 - (1.77 \times 6.2)$

$V_{DS} = 9.026V.$

67) The circuit shown in fig represents a small signal such that V_o is 20 times V_s is Amplitude. Find the Necessary

Value for Rs if $I_D = 15mA$ when $V_{GS} = 4V$ and $V_p = 2V$.



Hint: Voltage divider Bias

Soln:-

$$V_{GS} = V_G - I_D R_S$$

($V_{GS} \Rightarrow 4$)

$$V_G = \frac{10 \times 25}{10 + 30}$$

$$V_{GS} = \frac{10 \times 25}{10+30} - 15 \times 10^{-3} \times R_S$$

$$\therefore R_S = 150\ \Omega.$$

68) Determine the source to drain voltage required to bias a p-channel enchancement-mode MOSFET in the saturation region. Given $K_p = 0.2mA/V^2$, $V_{TP} = -0.50V$ and $I_D = 5mA$

Soln:- To find V_{SD}:-

a) To find I_D:- $I_D = K_p[V_{GS} - V_{TP}]^2$

$$0.5 \times 10^{-3} = 0.2 \times 10^{-3}[V_{SG} - 0.50]^2$$

$$2.5 = V_{SG}^2 - V_{SG} + 0.25$$

$$V_{SG}^2 - V_{SG} - 2.25 = 0.$$

$$V_{SG} = \frac{-(-1) \pm \sqrt{(-1)^2 - 4(1)(-2.25)}}{2(1)}$$

$$= \frac{1 \pm \sqrt{10}}{2}$$

$V_{SG} = 2.08V$ (or) $-1.08V$.

$V_{SG} = 2.08V$.

To find p-channel MOSFET in Saturation region,

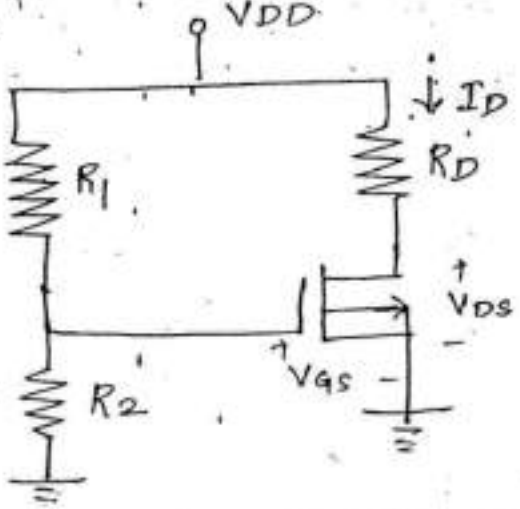
$V_{SD} > V_{SD(sat)} \Rightarrow V_{SG} + V_{TP} \Rightarrow 2.08 - 0.5$

$V_{SD} = 1.58V$.

69) Calculate the drain current and drain to source of a common source circuit with an n-Channel E-Mos

Circuit shown in fig. Assume that η_1 = [illegible]
$R_2 = 20K\Omega$, $R_D = 10K\Omega$, $V_{DD} = 6V$, $V_{GS(Th)} = 1V$ a
$K = 0.2mA/V^2$. (B)

Q:-



Hint:- Voltage divider Bias.

Soln:- i) V_G :- $V_G = V_{GS} \Rightarrow \frac{R_2}{R_1+R_2} \times V_{DD}$

$$= \frac{20\times10^3}{(30+20)\times10^3} \times 6$$

$$V_G = 2.4V$$

ii) I_D :- $I_D = K[V_{GS} - V_{GS(Th)}]^2$

$$= 0.2\times10^{-3}[2.4-1]^2$$

$$= 0.2\times10^{-3}[1.4]^2$$

$$I_D = 0.392mA$$

iii) V_{DS} :- $V_{DS} = V_{DD} - I_D R_D$

$$= 6 - (0.392\times10^{-3})(10\times10^3)$$

$$V_{DS} = 6 - 3.92$$

$$V_{DS} = 2.08V$$

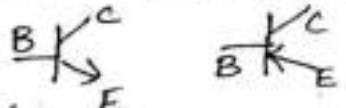
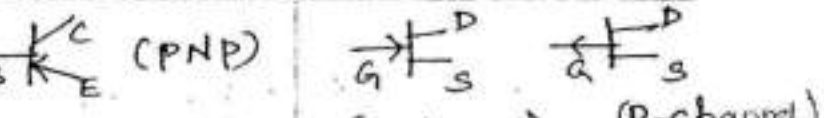
iv) P_T :- $P_T = I_D V_{DS}$

$$= (0.392\times10^{-3})(2.08)$$

$$P_T = 0.82mW.$$

*) Comparison of BJT and FET :-

Parameter	BJT	FET
i) Control element	Current Controlled device. Input current I_B controls I_C	Voltage controlled dev. Input Voltage V_{GS} Cont drain current I_D.

ii)	Device	Current flows due to both, Majority and Minority Carriers and hence bipolar device.	Current flows only due to Majority carriers and hence unipolar device.
iii)	Configuration	CE, CB, CC	CD, CS, CG
iv)	Input Resistance	Less	High
v)	Symbol	 (NPN) (PNP)	 (N-channel) (P-channel)
vi)	Gain	High	Low
vii)	Thermal Stability	Less	High
viii)	Size	Bigger	Smaller
ix)	Sensitivity	High	Less
x)	Ratio of o/p to i/p	$\beta = \frac{I_C}{I_B}$	$g_m = \frac{I_D}{V_{GS}}$

TOPIC 7: RECTIFIERS AND FILTERS

a) RECTIFIERS:-

→ The p-n junction diode conducts in one direction. It conducts when forward biased while practically it does not conduct when reverse biased.

→ Hence, it can be used to convert a.c supply to d.c supply.

→ A Rectifier is a device which converts a.c Voltage to pulsating d.c voltage, using one or more p-n junction diodes.

→ The p-n junction diode subjected to an a.c Voltage acts a rectifier converting Alternating Voltage to a pulsating d.c voltage.

→ Types of Rectifiers using diodes are:

i) Half wave ii) Full wave iii) Bridge Rectifier

Cascode Amplifier

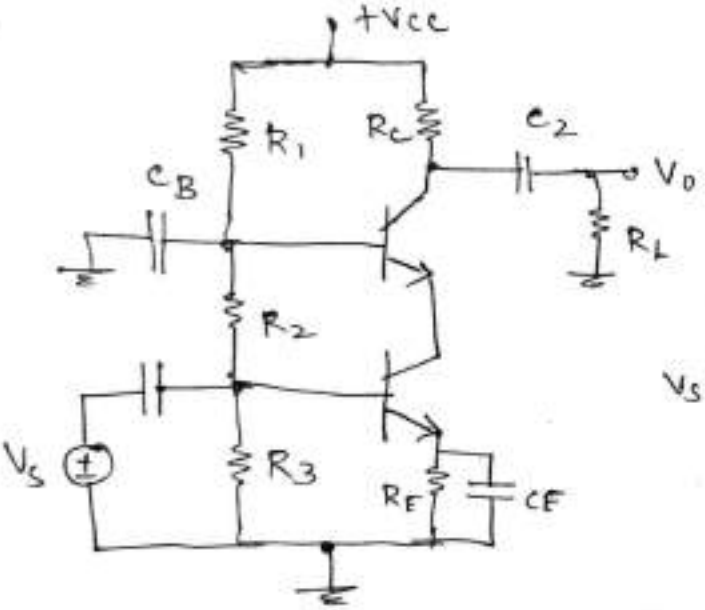
→ consists of common emitter in series with common base

Features:

1. It provides high input impedance, high voltage gain
2. provides improved input-output isolation as there is no direct coupling from o/p to i/p, eliminates miller effect & provides much B.W
3. provides very high o/p resistance, high slew rate, high stability

Disadv.

1) It requires two transistor & high supply voltage



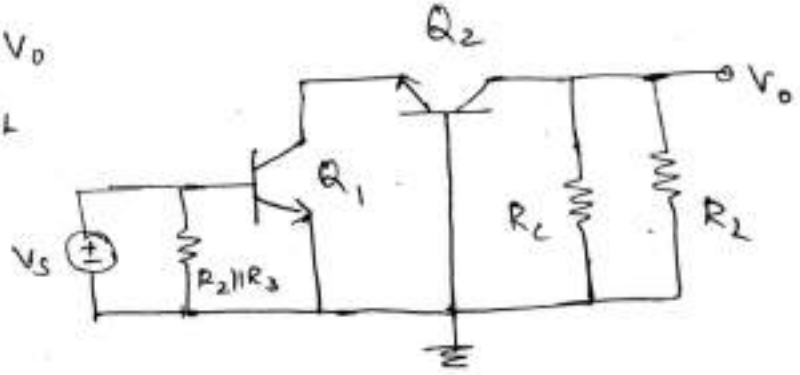
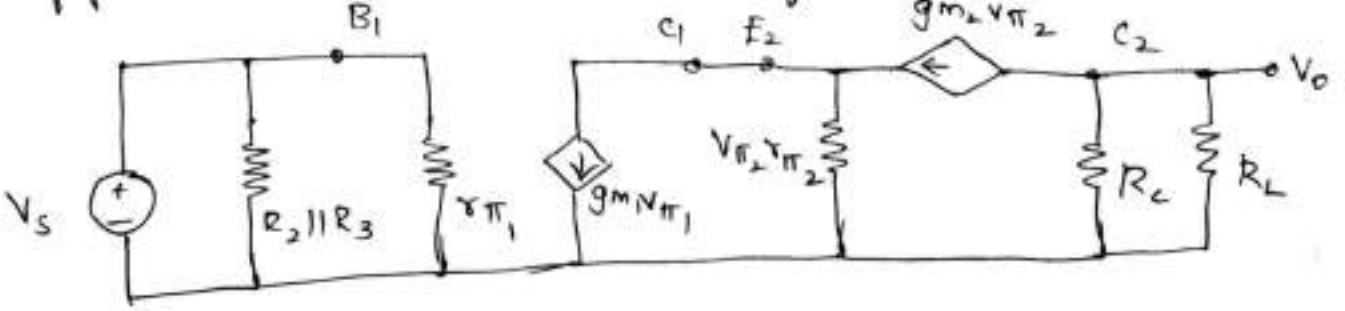


fig. shows a.c equivalent of CE - CB cascode amp.



Input impedance (R_i) = $R_2 \| R_3 \| r_{\pi_1}$

Output Impedance (R_o) = $R_c \| R_L$

Voltage gain (A_v):

$V_s = V_{\pi_1}$

Applying KCL at t_2

$$g_{m_1} V_{\pi_1} = \frac{V_{\pi_2}}{r_{\pi_2}} + g_{m_2} V_{\pi_2}$$

$$g_{m_1} V_s = \frac{V_{\pi_2}}{r_{\pi_2}} + g_{m_2} V_{\pi_2} \qquad \because V_s = V_{\pi_1}$$

$$g_{m_1} V_s = \frac{V_{\pi_2} + g_{m_2} V_{\pi_2} r_{\pi_2}}{r_{\pi_2}} = \frac{V_{\pi_2}(1+\beta_2)}{r_{\pi_2}} \qquad \because g_m r_\pi = \beta$$

$$V_{\pi_2} = \frac{r_{\pi_2}}{(1+\beta_2)} (g_{m_1} V_s) \quad \text{—(8)}$$

Output voltage V_o is given by

$$V_o = -(g_{m_2} V_{\pi_2})(R_c \| R_L) \quad \text{—(9)}.$$

sub (8) in (9)

$$V_o = -g_{m_2}(g_{m_1} V_s)\left(\frac{r_{\pi_2}}{1+\beta_2}\right)(R_c \| R_L)$$

$$\boxed{A_v = \frac{V_o}{V_s} = -g_{m_1} g_{m_2} \left(\frac{r_{\pi_2}}{1+\beta_2}\right)(R_c \| R_L)}$$

$$A_v = -g_{m_1} \left(\frac{g_{m_2} r_{\pi_2}}{1+\beta_2}\right)(R_c \| R_L)$$

$$\boxed{A_v = -g_m (R_c \| R_L)}$$

$\because g_{m_2} r_{\pi_2} = \beta_2$

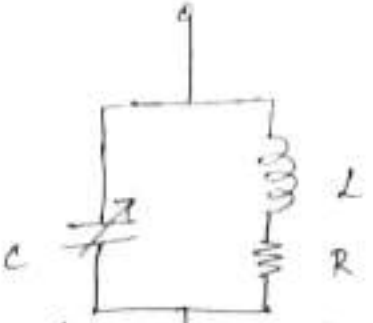
$$\frac{\beta_2}{1+\beta_2} \cong 1$$

Unit - IV

Tuned Amplifiers

To amplify selective range of freq Rc replaced by tuned ckt

→ A tuned parallel LC circuit resonates at a particular freq f_0.



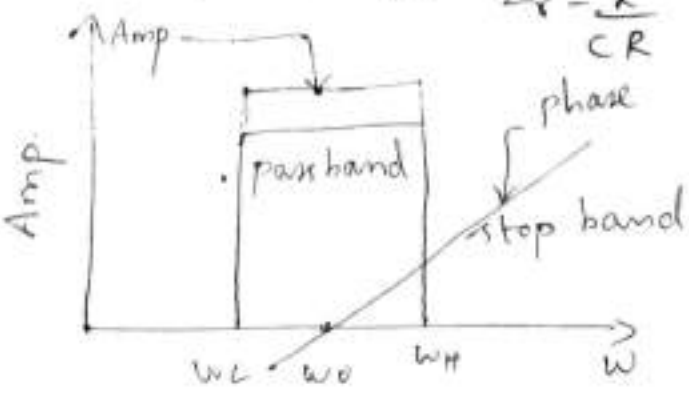
→ The response of tuned amplifiers is max. at resonant freq & falls below below value to

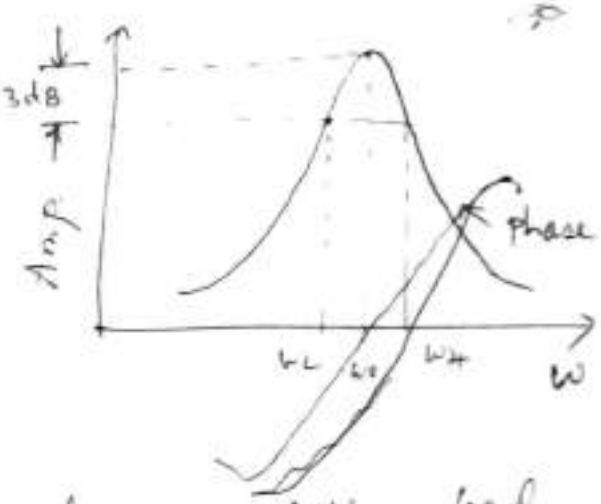
→ Tuned amplifier amplifies signals within narrow freq band centered about f_0.

→ The resonant freq. of the circuit is given as

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \quad \text{or} \quad \omega_0 = \frac{1}{\sqrt{LC}}.$$

$$Z_r = \frac{L}{CR}$$





→ At resonance, tuned ckt is used as resistive load as $X_L = X_C$, and reactance part becomes zero.

→ The ckt acts as pure resistive with V & I in phase

→ for freq. > fo, the ckt. is capacitive, I leads V

→ for freq. < fo, the ckt is inductive, I lags V

→ gain is $\propto Z_L$

→ Tuned amp. are used for amplification of narrow band of freq.

coil losses:

→ Tuned ckt consists of coil

→ coil is not purely inductive → leakage resistance in series with inductor

→ total loss = Cu loss + eddy current loss + hysteresis loss

→ Cu loss ↓ d.c resistance of coil → ½ f

eddy current loss ↓ I flowing in copper or core cased by induction heating within inductors, Cu or core → $\propto f$

hysteresis loss ↓ area of hysteresis loop → rate at which it is traversed indep. of freq. — energy lost as heat in traversing a magnetic material

Q factor:

The lower the value of resistance in inductor better is the Q.

Q factor → ratio of impedance of coil to its resistance

$$Q = 2\pi \times \frac{\text{max. energy stored per cycle}}{\text{Energy dissipated per cycle}}$$

Energy stored in cap. $= \frac{1}{2} C V_{max}^2$ → max value of volt across capacitor

$R << \frac{1}{\omega C}$

$V_{max} = \frac{I_m}{\omega C}$ → max value of I throu' C & R

$= \frac{1}{2} C V_{max}^2 = \frac{1}{2} \frac{I_m^2}{\omega^2 C}$

Energy dissipated per cycle $= \frac{I_m^2 R}{2f}$

$$Q = 2\pi \times \frac{\frac{I_m^2}{2\omega^2 C_s}}{\frac{I_m^2 R_s}{2f}} = 2\pi \times \frac{I_m^2}{2\omega^2 C_s} \times \frac{2f}{I_m^2 R_s}$$

$$= \frac{2\pi \times I_m^2 \times 2f}{2 \times (2\pi f)^2 C_s \times I_m^2 R} = \frac{1}{2\pi f \times C \times R} = \frac{1}{\omega C R}.$$

Unloaded & Loaded Q

→ When tank ckt is not connected to external circuit or load, Q accounts for internal losses and known as unloaded quality factor Q_u.

$$Q_u = 2\pi \times \frac{\text{max. energy stored per cycle}}{\text{Energy dissipated per cycle in tank ckt}}$$

→ when tank circuit is connected to load, the quality factor Q_L is

$$Q_L = 2\pi \times \frac{\text{max. energy stored per cycle}}{\text{Energy dissipated per cycle in tank ckt} + \text{Energy dissipated per cycle due to presence of external load}}$$

I_m is the peak value of current

→ max energy stored per cycle

$$= \frac{1}{2} L I_m^2$$

→ average power dissipated in inductor per cycle

$$= \left(\frac{I_m}{\sqrt{2}}\right)^2 R$$

Energy = power x time

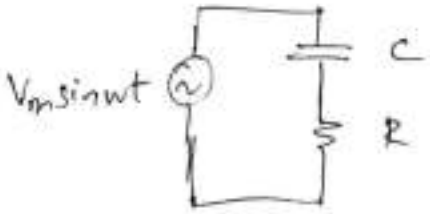
Energy dissip. per cycle = power x periodic time for one cycle

$$= \left(\frac{I_m}{\sqrt{2}}\right)^2 R \times T$$

$$= \frac{I_m^2}{2} R T = \frac{I_m^2}{2} \frac{R}{f}$$

$$Q = 2\pi \times \frac{\frac{1}{2} L I_m^2}{\frac{I_m^2 R}{2f}} = \frac{\omega L}{R} = \frac{X_L}{R}$$

Q factor for capacitor

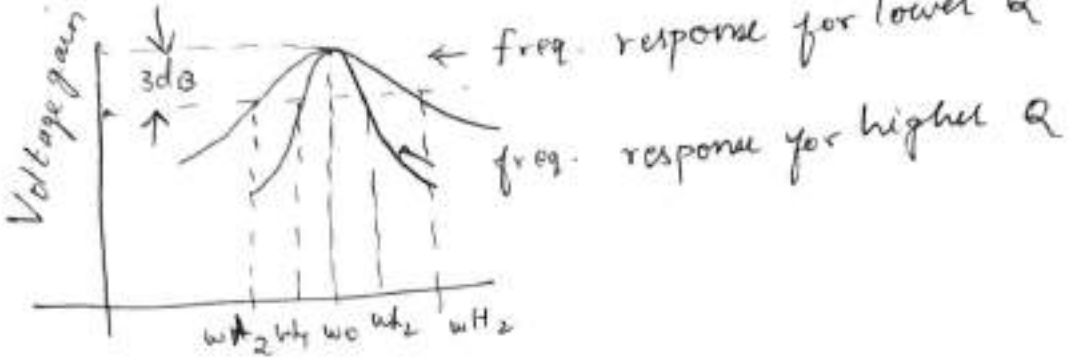


Gain and Frequency response

- determines 3dB Bandwidth for resonant ckt.

$$B.W = \frac{f_r}{Q} \rightarrow \text{represents centre freq.}$$

for higher Q values B.W is reduced.



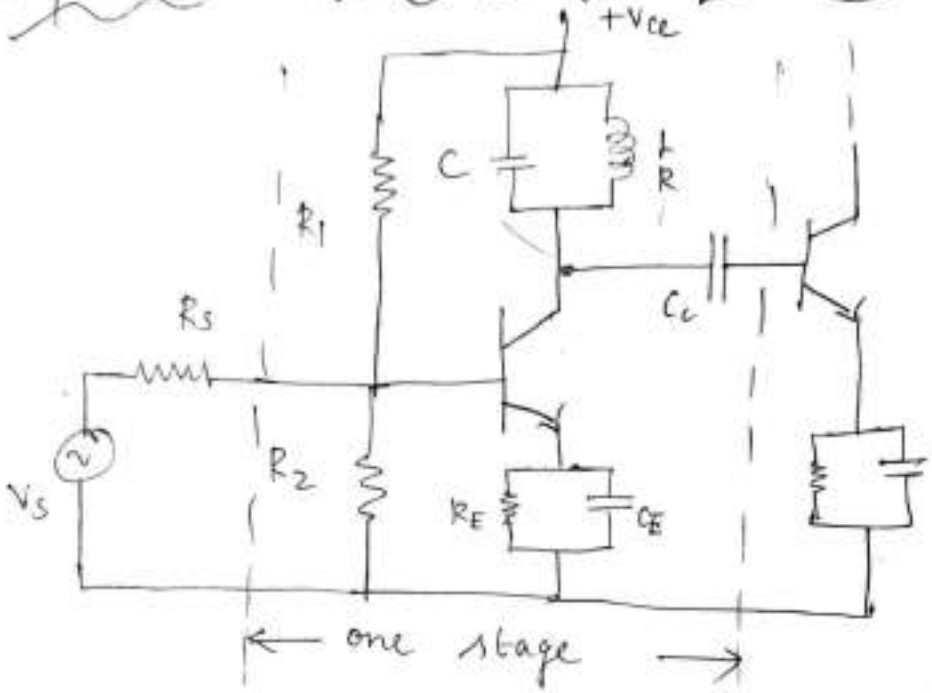
Small signal Tuned Amplifier

→ To obtain large voltage gain, it is required to use number of tuned amplifier stages in cascade

→ Cascade Tuned amplifier

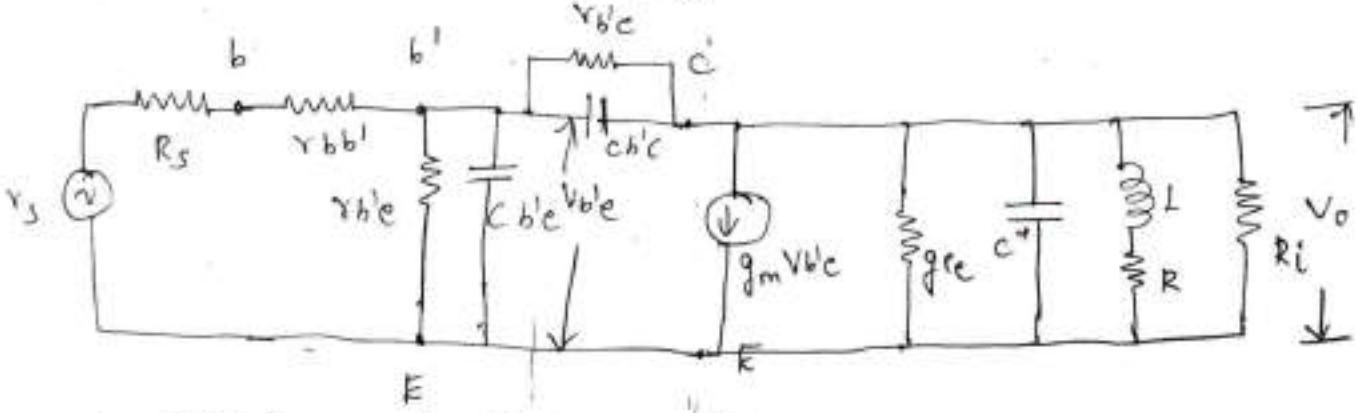
- Single tuned (one parallel resonant as load impedance & all tuned circuits are tuned to same freq)
  - capacitance coupled
  - transformer coupled or inductively coupled
- double tuned (two inductively coupled tuned ckts per stage both tuned to same freq)
- Stagger tuned (no. of single tuned stages in cascade successive tuned ckts tuned to slightly different freq).

Analysis of Capacitance coupled Single Tuned Amplifier

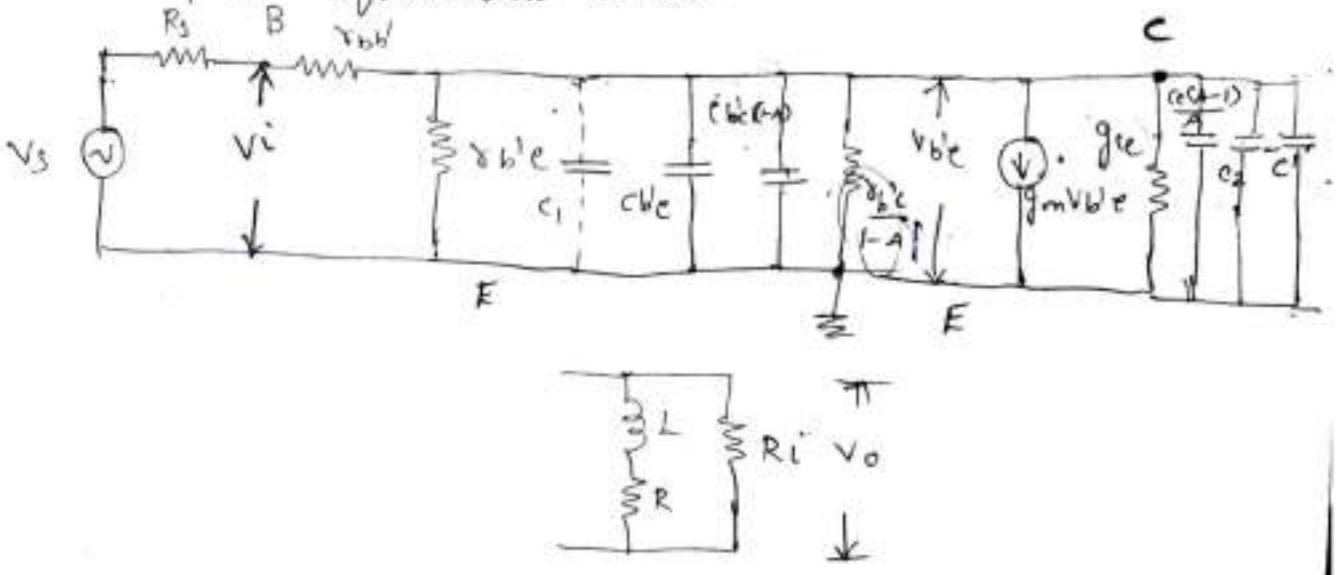


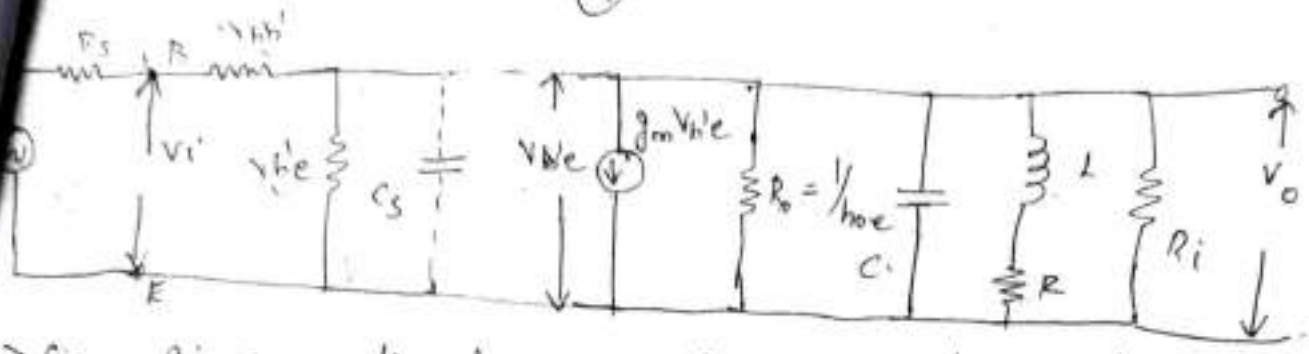
→ o/p across tuned ckt is coupled to next stage thro' C_c.

The equivalent ckt using hybrid π model is,



modified equivalent circuit





→ fig. gives modified equivalent ckt by applying Miller Theorem

→ A voltage gain, C_1, C_2 – stray wiring capacitances

→ all capacitances in i/p can be grouped to form C_s

$$C_s = C_{b'c} + C_1 + C_{b'c}(1-A)$$

→ all capacitances at o/p is grouped to

$$C = C_{b'c}\left(\frac{A-1}{A}\right) + C_2 + C'$$

$$g_{ce} = \frac{1}{r_{ce}} = h_{oe} - g_m h_{re} \Rightarrow h_{oe} = \frac{1}{R_o} \rightarrow \text{o/p resistance}$$

→ The reactance of by pass & coupling capacitor are negligibly small at operating freq and neglected.

Admittance of inductor along with resistor R is,

$$Y = \frac{1}{R+j\omega L} = \frac{R-j\omega L}{(R+j\omega L)(R-j\omega L)} = \frac{R-j\omega L}{R^2+j\omega^2 L^2}$$

$$= \frac{R}{R^2+\omega^2 L^2} - j\frac{\omega L}{(R^2+\omega^2 L^2)}$$

$$= \frac{1}{R_p} + \frac{1}{j\omega L_p}$$

where $R_p = \frac{R^2+\omega^2 L^2}{R}$ and $L_p = \frac{R^2+\omega^2 L^2}{\omega^2 L}$

The inductor is represented by R_p & L_p

Q of the coil $Q_0 = \frac{\omega_0 L}{R}$

where $\omega_0 = \frac{1}{\sqrt{LC}}$ is freq of resonance of ckt

Q_0 of coil is large $\omega L >> R$ in freq range of operation.

As $\frac{R}{\omega^2 L^2} << 1$,, $R_p = \frac{R^2 + \omega^2 L^2}{R} = \frac{R\left(R + \frac{\omega^2 L^2}{R}\right)}{R}$ $R_p = \frac{\omega L}{R}$

$$L_p = \frac{R^2 + \omega^2 L^2}{\omega^2 L}$$

÷ Nr & Dr terms by $\omega^2 L$

$$L_p = \frac{\frac{R^2}{\omega^2 L} + L}{1}$$

$\therefore \omega L >> R$

$$L_p \cong L$$

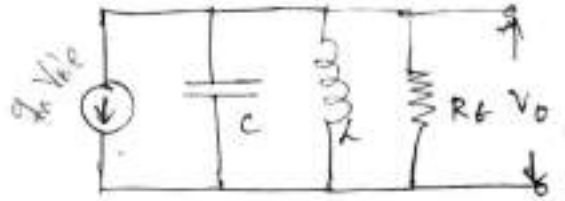
The o/p ckt of amplifier

R_t in parallel combination of R_o, R_p & R_i ie.

$$\frac{1}{R_t} = \frac{1}{R_o} + \frac{1}{R_p} + \frac{1}{R_i}$$

The effective Q factor

$$Q_e = \frac{\text{susceptance of inductance } L \text{ or } C}{\text{conductance of shunt resistance } R_t}$$



$$Q_e = \omega_0 C R_t = \frac{R_t}{\omega_0 L}$$

from o/p

$$V_o = -g_m V_{b'e} Z$$

Z is impedance of C, L and R_t in parallel.

$Y = 1/Z$ is

$$Y = \frac{1}{Z} = \frac{1}{R_t} + \frac{1}{j\omega L} + j\omega C$$

$$= \frac{1}{R_t}\left[1 + \frac{R_t}{j\omega L} + j\omega C R_t\right]$$

y/y Nr. & Dr by ω_0

$$Y = \frac{1}{R_t}\left[1 + \frac{R_t \omega_0}{j\omega L \omega_0} + \frac{j\omega \omega_0 C R_t}{\omega_0}\right]$$

$$\frac{R_t}{\omega_0 L} = \omega_0 C R_t = Q_e$$

$$Y = \frac{1 + jQ_e\left[\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right]}{R_t}$$

$$Z = 1/Y = \frac{R_t}{1 + jQ_e\left[\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right]}.$$

'δ' indicate fractional freq. Variation

$$\delta = \frac{\omega - \omega_0}{\omega_0} = \frac{\omega}{\omega_0} - \frac{\omega_0}{\omega_0} = \frac{\omega}{\omega_0} - 1$$

$$\frac{\omega}{\omega_0} = 1 + \delta$$

$$Z = \frac{R_t}{1 + jQ_e\left[(1+\delta) - \frac{1}{(1+\delta)}\right]}$$

SIMD Instruction set Extension for multimedia

→ graphic system used 8 bits to represent three primary colours

→ By partitioning

$$= \frac{R_t}{1+jQ_e\left[\frac{1+\delta^2+2\delta-1}{(1+\delta)}\right]} = \frac{R_t}{1+j2\delta Q_e\left[\frac{\delta/2+1}{1+\delta}\right]}$$

At any freq ω is close to ω_0, $\delta << 1$ ($\because \omega - \omega_0 << 1$

$$Z = \frac{R_t}{1+j2Q_e\delta}$$

At resonance $\omega = \omega_0$ & $\delta = 0$. The impedance Z becomes

$$Z = R_t = R_0 \| R_p \| R$$

$$R_p = \frac{\omega_0^2 L^2}{R} = \frac{\omega_0 L}{\omega_0 CR} \quad \left(\because \omega_0 L = \frac{1}{\omega_0 C}\right)$$

$$= \frac{L}{CR}$$

At resonance, R_p can be expressed as

$$R_p = \frac{\omega_0^2 L^2}{R}$$

$$Q_0 = \frac{\omega_0 L}{R}$$

$$Q_0^2 = \frac{\omega_0^2 L^2}{R^2}$$

$$R_p = Q_0^2 R = \omega_0 L Q_0$$

where Q_0 is Q of the coil alone at resonance.

from fig neglecting C_s

$$V_{b'e} = V_i \frac{r_{b'e}}{r_{bb'} + r_{b'e}}$$

$$V_o = -g_m V_{b'e} Z$$

$$= -g_m \left[V_i \frac{r_{b'e}}{r_{bb'} + r_{b'e}} \right] Z$$

Voltage gain without considering source resistance is

$$A = \frac{V_o}{V_i} = -g_m \left(\frac{r_{b'e}}{r_{bb'} + r_{b'e}} \right) Z \quad R_t$$

$$\frac{}{1 + 2j Q_{eff} \delta}$$

Voltage gain at resonance ($\delta = 0$)

$$A_{res} = -g_m \left(\frac{r_{b'e}}{r_{bb'} + r_{b'e}} \right) R_t$$

$R_t = R_0 \| R_p \| R_{in}$

$$\frac{A}{A_{res}} = \frac{1}{1 + j 2 \delta Q_{eff}}$$

$$\left| \frac{A}{A_{res}} \right| = \frac{1}{\sqrt{1 + (2 \delta Q_e)^2}}$$

Phase angle $\frac{A}{A_{res}}$ is given by

$$\phi = \tan^{-1} (2 \delta Q_e)$$

At freq ω_t below resonant freq

$$\delta = \frac{1}{2 Q_e}$$

$$\left| \frac{A}{A_{res}} \right| = \frac{1}{\sqrt{2}} = 0.707$$

gain A is 3 dB lower than A_{res}.

freq w_1 is lower 3 dB freq

at freq w_2 above w_0,

$$\delta = \pm \frac{1}{2Q_e}$$

$$\left|\frac{A}{A_{res}}\right| = \frac{1}{\sqrt{2}} = 0.707$$

w_2 is upper 3 dB freq.

Δw or $BW = w_2 - w_1$

$$\Delta w = \frac{[(w_2 - w_0) + (w_0 - w_1)]w_0}{w_0}$$

$$= \left[\frac{(w_2 - w_0)}{w_0} + \frac{w_0 - w_1}{w_0}\right] w_0 = [\delta + \delta] w_0$$

$$\Delta w = 2\delta w_0$$

$$\delta = \frac{1}{2Q_e}$$

$$2\delta = \frac{1}{Q_e}$$

$$\Delta w = \frac{w_0}{Q_e}$$

from (13.18) $Q_e = w_0 C R_t = \frac{R_t}{w_0 L}$

$$\Delta w = \frac{w_0}{R_t w_0 C} = \frac{1}{R_t C} \text{ rad/s.}$$

→ In single tuned amplifier 3dB B.W is $\frac{\omega_0}{Q}$

→ In double tuned amplifier B.W exceeds in single tuned by $\sqrt{(b^2-1) \pm 2b}$

→ b is +ve for practical ckt. $b < 0.414$ no real values of B.W

→ increase in b 3dB B.W of double tuned ↑. overshoot also increases

→ adv. large 3dB B.W than STA, & GBW, it provides Gain Vs freq curves steeper than flatter top

Effects of cascading single tuned Amp. on B.W

→ high gain, identical stages can be cascaded

→ overall Av is product of individual stages

→ high Av accompanied by narrow B.W

relative gain w.r.to gain at resonant freq fo

$$\left|\frac{A}{A_{res}}\right| = \frac{1}{\sqrt{1+(\delta Q_e)^2}}$$

for n stage

$$\left|\frac{A}{A_{res}}\right|^n = \left[\frac{1}{\sqrt{1+(2\delta Q_e)^2}}\right]^n$$

gain A is 3 dB lower than

→ 3dB freq for n stage cascade amplifier

by equating $\left|\frac{A}{A_{mid}}\right|^n$ to $\frac{1}{\sqrt{2}}$

$$\left[\frac{1}{\sqrt{1+(2\delta Q_e)^2}}\right]^n = 1/\sqrt{2} \qquad \left[1+(2Q_e\delta)^2\right]^{n} = 2^{1/n}$$

Squaring & Taking nth root $(2\delta Q_e)^2 = 2^{1/n}$

$$\left[1+(2\delta Q_e)^2\right]^{n/2} = 2^{1/2}$$

$$2\delta Q_e = \pm\sqrt{2^{1/n}-1}$$

Sub $\delta = \frac{\omega-\omega_0}{\omega_0}$, fractional freq. variation

$$2\left(\frac{f-f_0}{f_0}\right)Q_e = \pm\sqrt{2^{1/n}-1}$$

$$2(f-f_0)Q_e = \pm f_0\sqrt{2^{1/n}-1}$$

$$f_2 - f_0 = +\frac{f_0}{2Q_e}\cdot\sqrt{2^{1/n}-1}$$

$$f_0 - f_1 = +\frac{f}{2Q_e}\sqrt{2^{1/n}-1}$$

B.W of n stage identical amplifier is

$$B_{1n} = f_2 \sim f_1 = (f_2-f_0) + f_0 - f_1$$

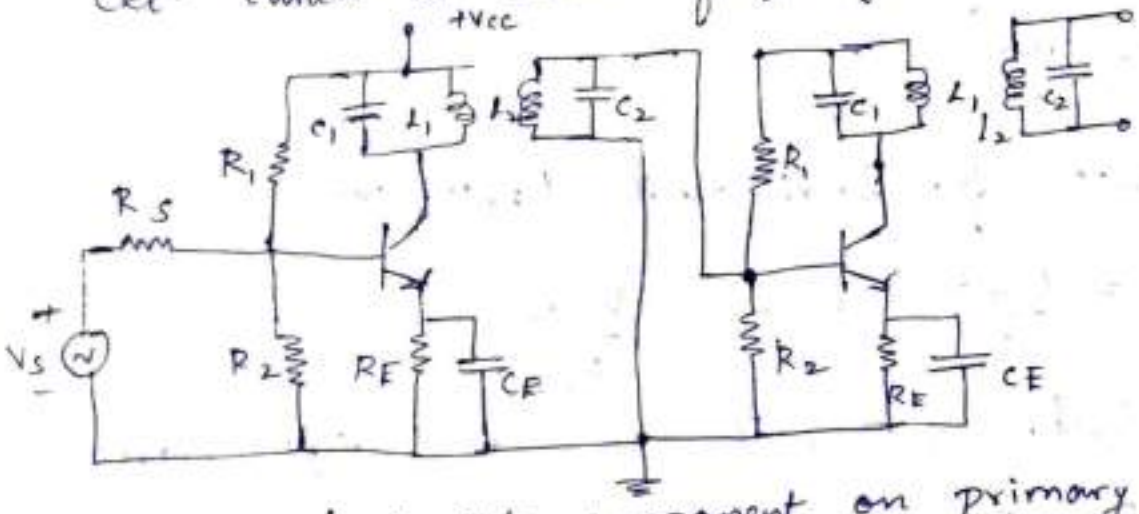
$$= \frac{f_0}{2Q_e}\sqrt{2^{1/n}-1} + \frac{f_0}{2Q_e}\sqrt{2^{1/n}-1}$$

$$= \frac{f_0}{Q_e}\sqrt{2^{1/n}-1}$$

$$= B_1\sqrt{2^{1/n}-1}$$

Double Tuned Amplifier:

→ Voltage developed across tuned circuit is coupled inductively to another tuned circuit. Both Tuned ckt tuned to same frequency.



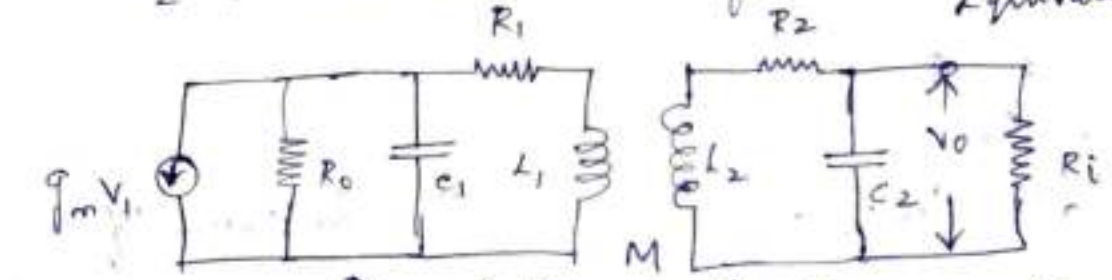
$L_1 C_1$ → tank ckt component on primary side

$L_2 C_2$ → tank ckt components on secondary side

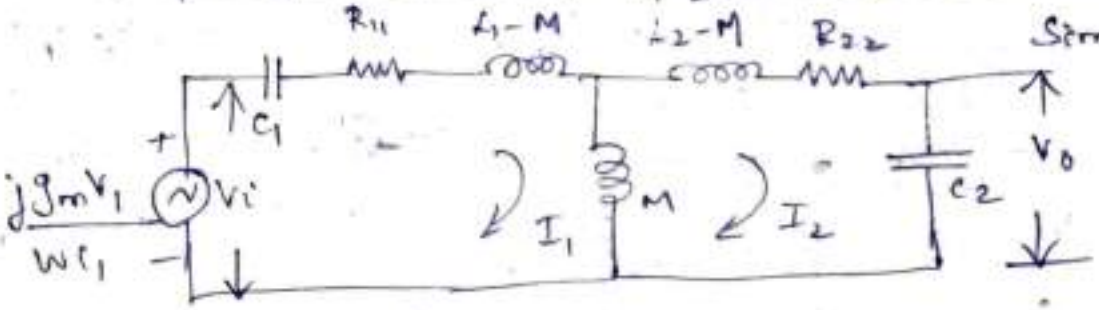
R_1 → series resistance of inductance L_1

R_2 → series resistance of inductance L_2

Equivalent ckt



Simplified Equivalent ckt.



$$R_{11} = \frac{\omega_0^2 L_1^2}{R_0} + R_1$$

$$R_{12} = \frac{\omega_0^2 L_2^2}{R_i} + R_2$$

gain A_i.

In simplified ckt current source replaced by voltage source which is in series with C_1.

→ & also effect of mutual inductance on primary & secondary side

$$Q = \frac{\omega_r L}{R}$$

Q factor for individual tank ckt

$$Q_1 = \frac{\omega_r L_1}{R_{11}} \quad \& \quad Q_2 = \frac{\omega_r L_2}{R_{22}}$$

Q factor for both ckt are kept same

$$Q_1 = Q_2 = Q$$

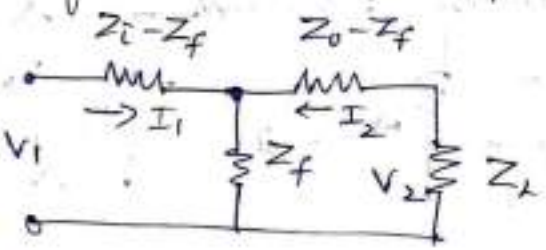
resonant frequency $\omega_r^2 = 1/L_1C_1 = 1/L_2C_2$

The o/p voltage can be given as

$$V_0 = \frac{-j}{\omega_r C_2} I_2$$

To calculate V_0/V_1 → represent I_2 interms of V_1

Find transfer admittance Y_T.



$(Z_i - Z_f) I_1 + Z_f (I_1 - I_2) = V_1$

$Z_i I_1 - Z_f I_2 = V_1$

$Z_i I_1 - Z_f I_2 = V_1$

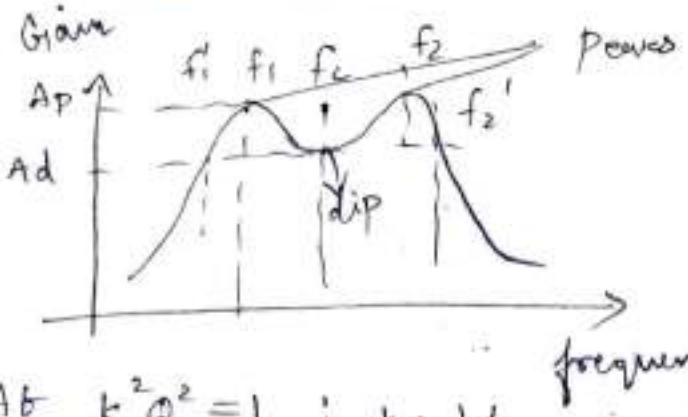
$$Y_T = \frac{I_2}{V_1} = \frac{I_2}{I_1 Z_{11}} = \frac{A_i}{Z_{11}}$$

$$= \frac{Z_f}{Z_f^2 - Z_i(Z_0 + Z_L)}$$

$$Z_{11} = \frac{V_1}{I_1} = Z_i - \frac{Z_f^2}{Z_0 + Z_L}$$

$$A_i = \frac{I_2}{I_1} = \frac{-Z_f}{Z_0 + Z_L}$$

The simplified ckt is similar to



At $k^2Q^2 = 1$; $k = 1/Q$, $f_1 = f_2 = f_0$ → is called critical coupling

→ for $k < 1/Q$ peak gain is less than maximum gain & coupling is poor

→ At $k > 1/Q$, circuit over coupled → shows double peak with more B.W

→ gain magnitude at peak is

$$|A_p| = \frac{g_m w_0 \sqrt{L_1 L_2} * Q}{2}$$

→ gain at dip is

$$|A_d| = |A_p| \frac{2kQ}{1+k^2Q^2}$$

ratio of peak & dip gain is γ

$$\gamma = \left|\frac{A_p}{A_d}\right| = \frac{1+k^2Q^2}{2kQ}$$

$$kQ = \gamma + \sqrt{\gamma^2 - 1}$$

The B.W b/w freq at which gain is $|A_d|$ is useful B.W is

$$B.W = 2\delta' = \sqrt{2}\,(f_2 - f_1)$$

At 3dB $V = \sqrt{2}$

gain A is

At 3dB $\gamma = \sqrt{2}$

$$kQ = \gamma + \sqrt{\gamma^2 + 1} = \sqrt{2} + \sqrt{\sqrt{2}^2 + 1} = 2.414$$

3 dB B.W $= 2\delta' = \sqrt{2}(f_2 - f_1)$

$$= \sqrt{2}\left[f_r\left(1 + \frac{1}{2Q}\sqrt{k^2Q^2 - 1}\right) - f_r\left(1 - \frac{1}{2Q}\sqrt{k^2Q^2 - 1}\right)\right]$$

$$= \sqrt{2}\left(\frac{f_r}{Q}\sqrt{k^2Q^2 - 1}\right) = \sqrt{2}\frac{f_r}{Q}\sqrt{(2.414)^2 - 1} = \frac{3.1 f_r}{Q}$$

3 dB BW for single Tuned is $2f_r/Q$

" " " Double " is $3.1 f_r/Q$ > than single tuned.

$$\frac{w - w_0}{w_0} = \delta$$

$$\frac{w}{w_0} - \frac{w_0}{w_0} = \delta$$

$$\frac{w}{w_0} = \delta + 1$$

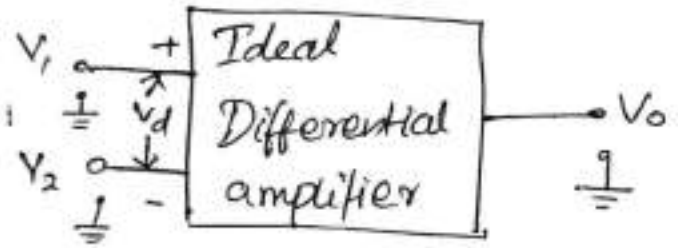
Differential Amplifier :-

→ A device which accepts an input Signal & produces an output Signal proportional to the input, is called an amplifier.

→ An amplifier which amplifies the difference between the two input signal is called differential amplifier.

Basics of Differential Amplifier:

→ consider an ideal differential amplifier



V_d = Difference input Signal

$= V_1 - V_2$

→ An ideal difference amplifier, the output voltage V_o is proportional to the difference between the two i/p Signal. Hence $V_o \propto (V_1 - V_2)$.

i) Differential Gain (A_d):

$$V_o = A_d (V_1 - V_2)$$

where A_d - constant of proportionality.

→ The A_d is the gain with which the differential amplifier amplifies the difference between two input Signal. Hence it is called differential gain of amplifier.

A_d - Differential Gain.

V_d - Difference Voltage

$V_o = A_d V_d$

$A_d = V_o / V_d$. $20 \log_{10}(A_d)$ in dB

ii) Common Mode Gain (A_c):

→ If we apply two input voltages which are equal in all the respects ie $V_1 = V_2$. then ideally $V_o = (V_1 - V_2) A_d = 0$

→ But practically, the difference amplifier also depends on the average common level of the two inputs.

→ The average level of the two input signal is called common mode signal, V_c

$$V_c = \frac{V_1 + V_2}{2}$$

→ The gain with which the differential amplifiers amplifies the common mode signal to produce the output is called common mode gain of the differential amplifier denoted as A_c

$$V_o = A_c V_c$$

→ The total output of any differential amplifier can be expressed as

$$V_o = A_d V_d + A_c V_c$$

Note: For an ideal differential amplifier

A_d = Infinite

A_c = Zero

$V_o = 0$

Practically

A_d - Very large

A_c - Not Zero (but very small)

iii) Common Mode Rejection Ratio (CMRR)

→ When $V_1 = V_2$, many disturbance signals, noise

signals appear as a common input signal to both input terminals which should be rejected.

→ " The ability of a differential amplifier to reject a common mode signal is expressed by a ratio called common mode rejection ratio, CMRR".

→ CMRR is defined as the ratio of the differential voltage gain A_d to common mode voltage gain A_c.

$$CMRR = \rho = \left|\frac{A_d}{A_c}\right|$$

→ Ideally $A_c = 0$ → CMRR is infinite.

→ Practically A_d - large, A_c - small, So CMRR is very large.

$$CMRR \text{ in } dB = 20 \log \left|\frac{A_d}{A_c}\right| \text{ dB}$$

→ output voltage in terms of CMRR.

$$V_o = A_d V_d + A_c V_c$$

$$= A_d V_d \left[1 + \frac{A_c V_c}{A_d V_d}\right]$$

$$= A_d V_d \left[1 + \frac{(V_c/V_d)}{(A_d/A_c)}\right]$$

$$V_o = A_d V_d \left[1 + \frac{1}{CMRR} \frac{V_c}{V_d}\right]$$

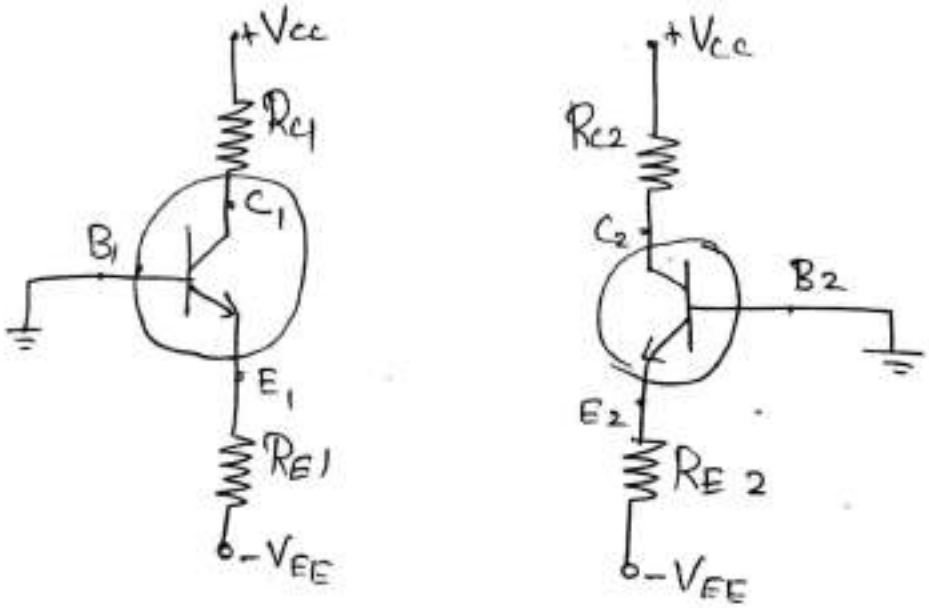
→ CMRR is very large, So if V_c & V_d both are present, the output is proportional to the difference signal only, the common mode component is greatly rejected.

Features of Differential Amplifier:

→ High differential Voltage gain
→ Low common mode gain
→ High CMRR
→ Two input terminals
→ High input impedance
→ Large bandwidth
→ Low offset Voltages & currents
→ Low output impedance

Transistorised Differential Amplifier:

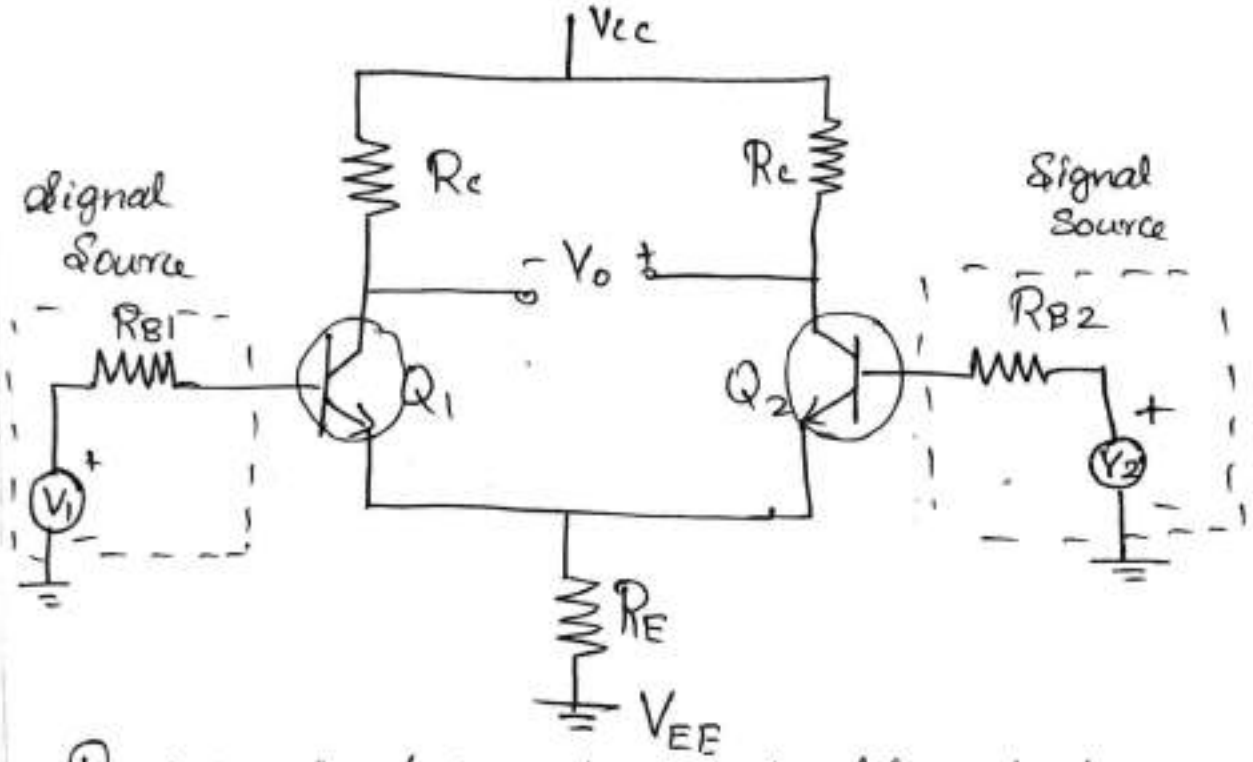
→ The transistorised differential amplifier uses the emitter biased circuits which are identical in characteristics.



→ Q_1 & Q_2 have matched characteristics.
Thus $R_{C1} = R_{C2} = R_C$, $R_{E1} = R_{E2}$, $|V_{CC}| = |V_{EE}|$

→ The differential amplifier can be obtained by connecting emitter of Q_1 to emitter of Q_2, Since now R_{E1} || to R_{E2}, we replace it with R_E.

→ Input V_1 is applied to B_1 & V_2 to B_2. The balanced output is taken across C_1 & C_2.
→ This amplifier is called emitter coupled differential amplifier.
→ Based upon, where the output is taken it is divided into two types.



Dual input, balanced output differential amplifier

Balanced output: double ended output or floating output is the output taken between two collectors, none of them is grounded.

Unbalanced output: or Single ended output is the output taken between any one of the collectors & the ground.

→ The circuit operation is mainly divided into two modes.

* Differential Mode Operation
* Common Mode Operation

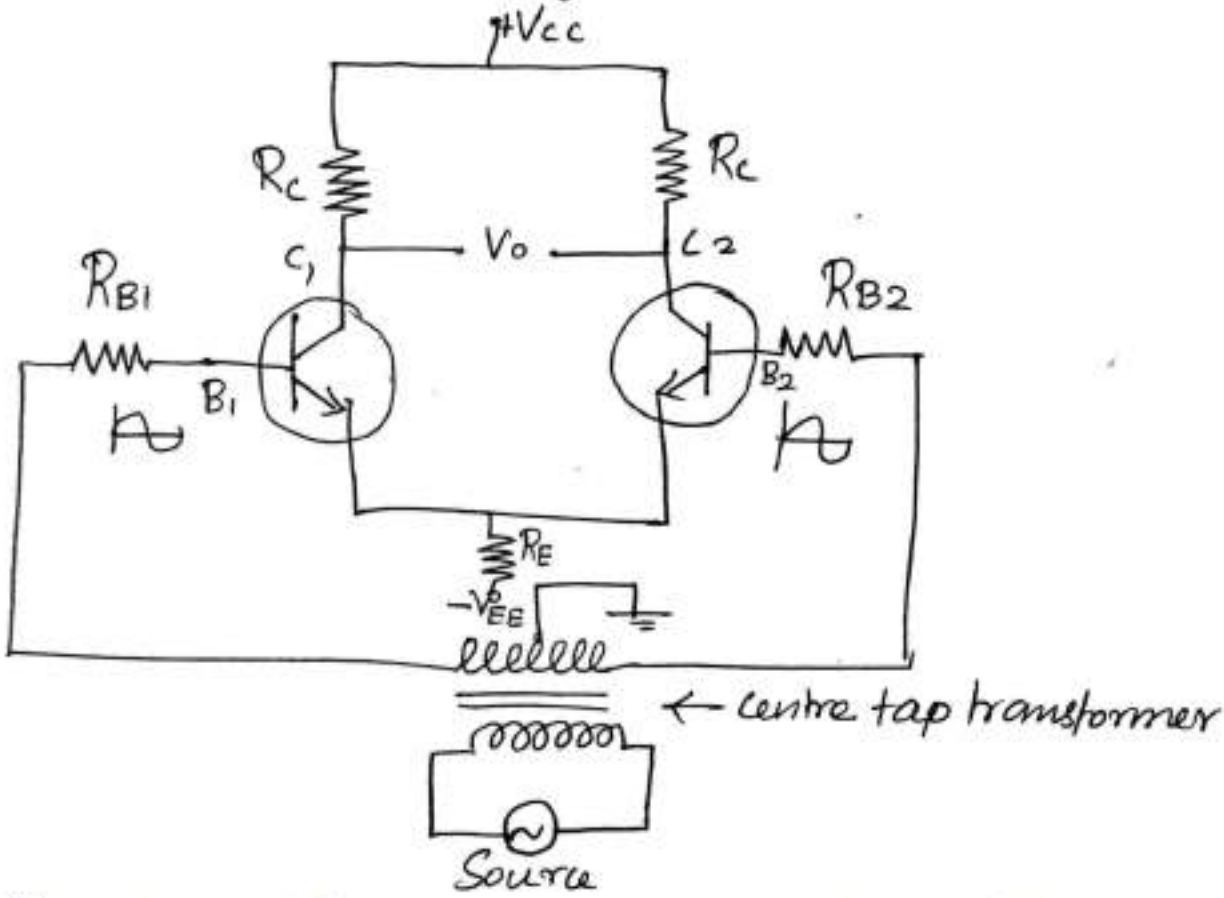
Differential Mode Operation:

→ In this mode, V_1 & V_2 are different from each other.

→ Consider V_1 is 180° out of phase with V_2, which can be obtained using center tap transformer.

→ Assume V_1 is +ve going on B_1 & negative going on Q_2.

→ with a +ve going signal on B_1, an amplified.



negative going signal develops on C_1 & due to +ve going signal, current through R_E also increases & a +ve going signal develops across R_E.

→ Similarly, when -ve going signal is applied at B_2 an amplified +ve going signal develops on C_2 & a -ve going signal develops across R_E.

→ Due to the effect of Q_1 & Q_2, the signal voltages at R_E are equal in magnitude but 180° out of phase.

→ The two signals cancel each other & there is no signal across R_E.

$$V_o = V_1 - V_2 \quad \text{Eg } +10 - (-10) = 20$$

→ Hence, the difference output, V_o is twice as large as signal voltage from either collector to ground.

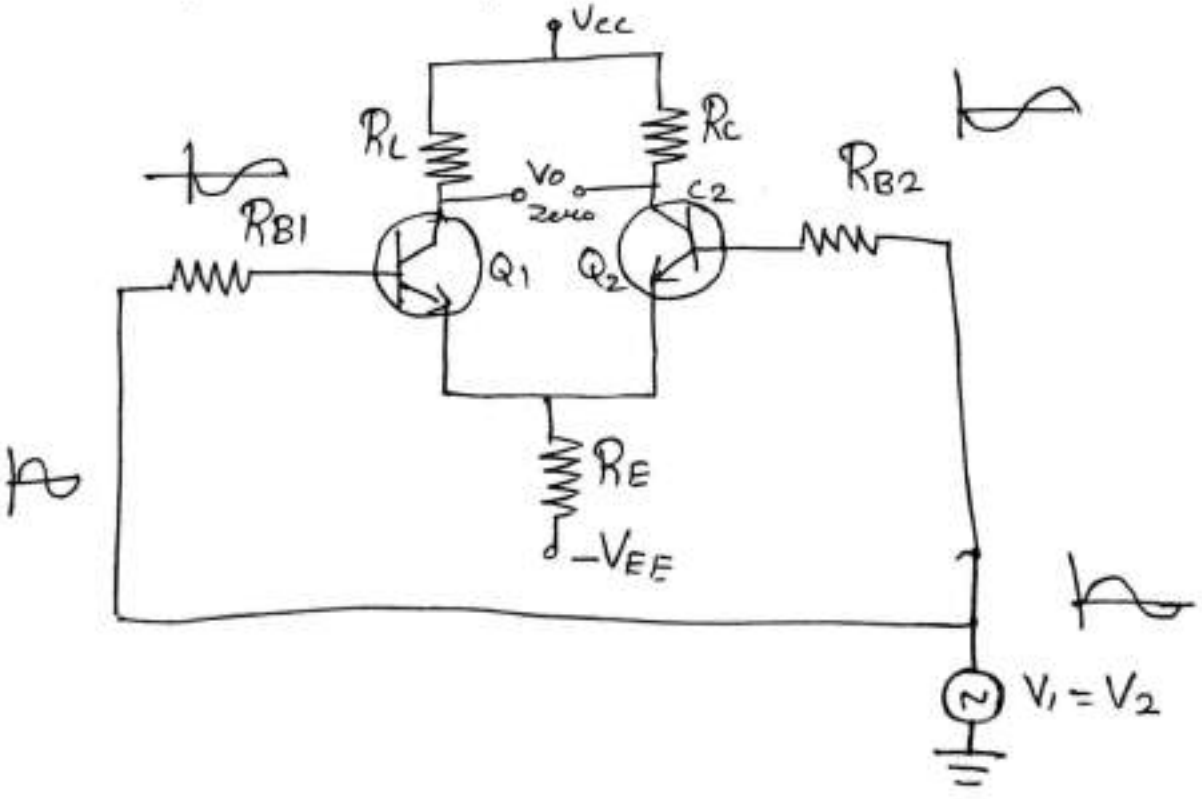
Common Mode Operation:

→ In this mode, $V_1 = V_2$ both in magnitude & phase

→ In phase signal voltages at the bases of Q_1 & Q_2 causes in phase signal voltages to appears across R_E which add together.

→ So, R_E provides negative feedback, which reduces A_c

→ The difference output V_o is almost zero.



Configurations of Differential Amplifier:

→ There are four configurations.

i) Dual input, balanced output differential Amplifier (DIBO)
ii) Dual input, unbalanced output differential Amplifier (DIUO)
iii) Single input, Balanced output differential Amplifier (SIBO)
iv) Sigle input, Unbalanced output differential Amplifier (SIUO)

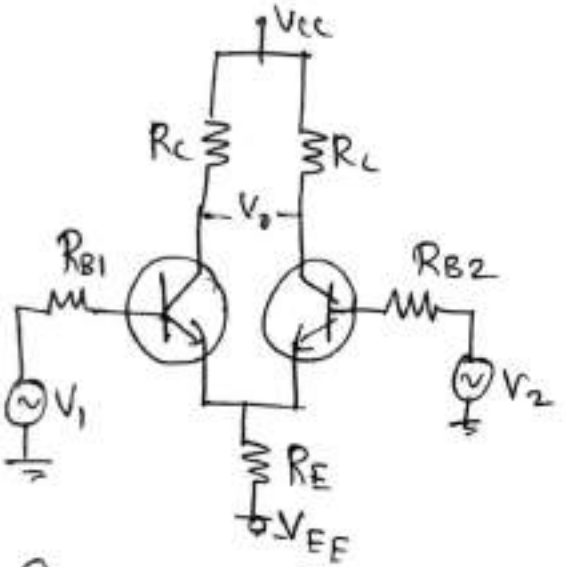
Differential amplifier

Balanced output: O/p taken between two collectors

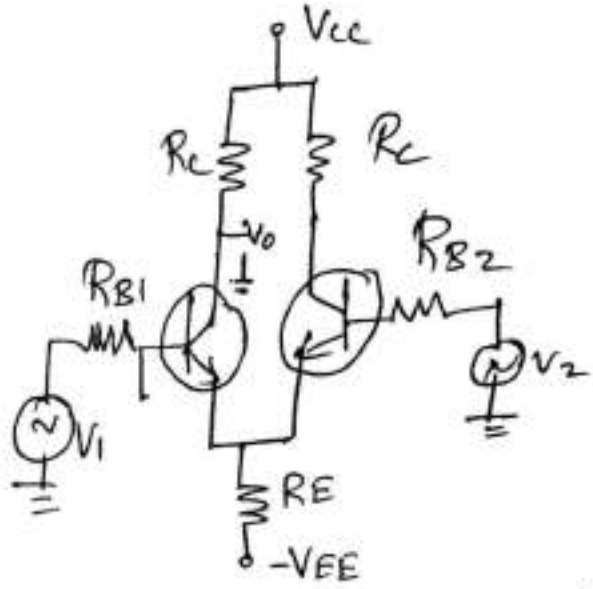
Unbalanced output: O/p taken between on collector with respect to ground.

Single input : Signal is given to one input terminal the other is grounded

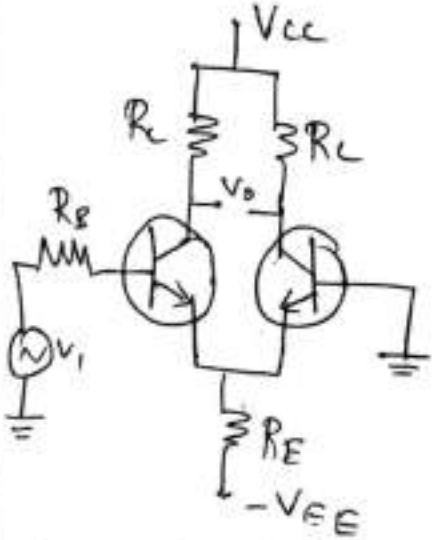
Double ended input : Signal is given to both the input terminal.



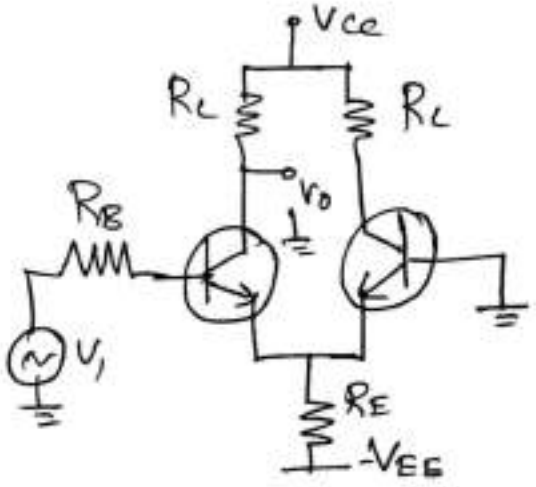
Dual input, balanced output



Dual input unbalanced output



Single input, balanced output



Single input, unbalanced output

→ A multistage amplifier with a desired voltage gain can be formed using a direct connection between successive stages of differential amplifier.

JET Input Stage:

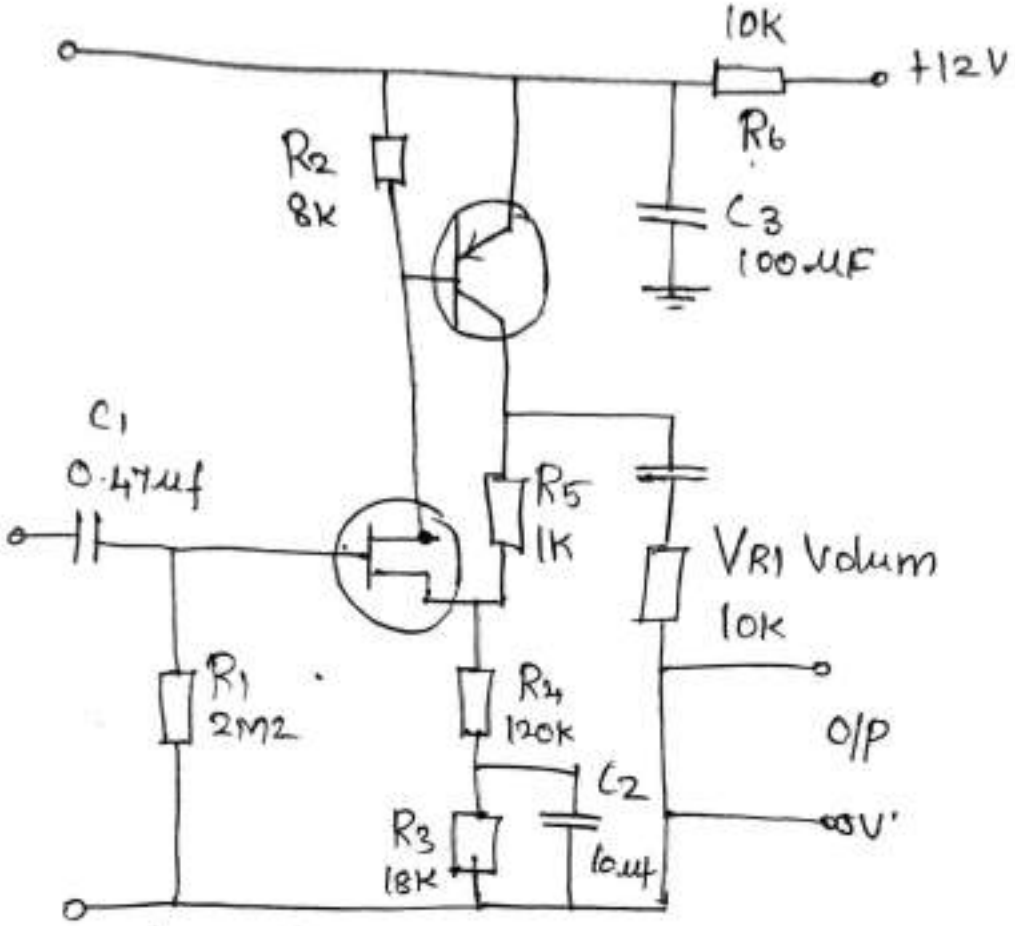


fig: high Impedance JFET Input Stage.

→ where very high impedance & low noise is required in an amplifier input, it is common to use a FET in an amplifier's input stage

→ Very high input impedance is obtainable with JFETs as its gate is voltage, rather than current operated.

→ Therefore the JFET takes hardly any current from the device connected to the amplifier input.

→ Even higher input impedance are available where MOSFETs with insulated gate construction (IGFETs) are used.

→ Although FETs generally have less voltage gain & less bandwidth than BJT transistors they also create much less internally generated noise, which makes them ideally suited for use in the early stages of an amplifier, where good signal to noise ratio is important.

Operation:

→ Because the input resistance of the JFET is extremely high, the input impedance of the circuit is approximately the value of R_1 & as practically no current is flowing into the input there is no potential across R_1, therefore the gate of transistor1 is effectively at zero volts.

→ To operate correctly, the gate of the N channel JFET must be more negative than the Source, this is achieved by making the Source of Transistor1 positive.

→ The biasing of the JFET is set by R_2 & R_3

→ As JFET gain is not particularly high, extra gain is provided by PNP transistor T_2

→ The overall gain of the two-stage amplifier is set at approximately 11 by the negative feedback provided by R_4 & R_5

Decoupling:

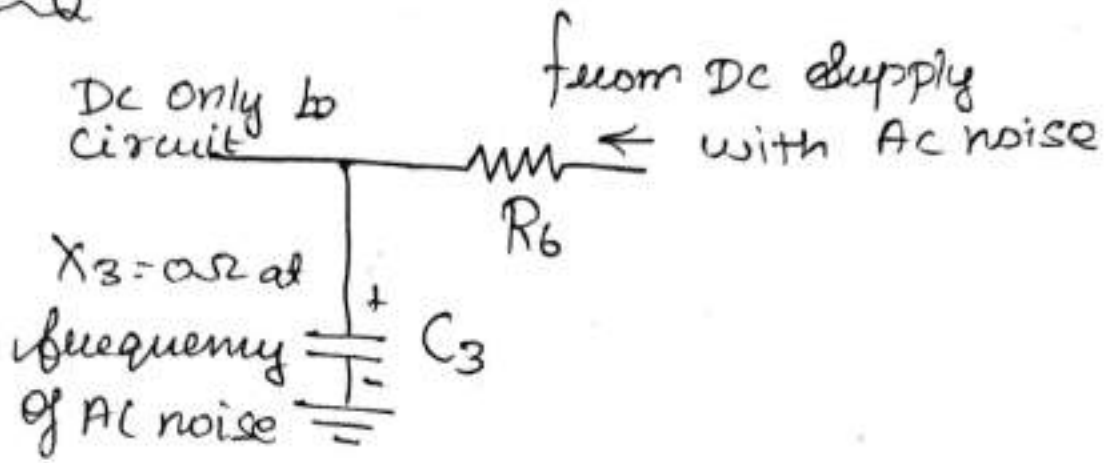


fig : Supply Decoupling

→ In the previous figure R_3 is decoupled by C_2 so that the bottom end of R_3 is effectively at ground potential as far as Ac is concerned, the value of C_2 is not particularly large in this circuit, as the larger the value of electrolytic capacitor the more noise it will produce, & the aim of the circuit is to keep internally generated noise to a minimum.

→ C_1 & C_4 coupling capacitors (also relatively small values) provide isolation from any Dc voltages present on any connected circuits.

→ Using a very high value for R_1 produces a high input impedance but the higher the value, the more prone the

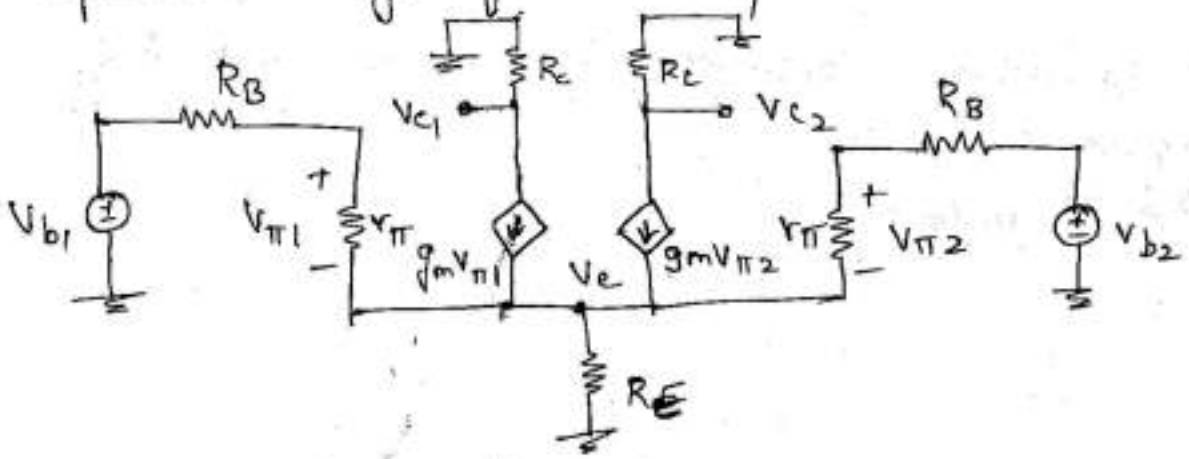
Differential ...

circuit will be to instability & oscillation,

→ To prevent this possibility, effective decoupling from other circuits & the supply is necessary, decoupling here is provided by R_6 & C_3 as shown in the figure.

Small Signal Analysis of Differential Amplifier

Assume early voltage $V_A = \infty$; $r_o = \infty$
constant current source is not ideal but represented by finite output resistance R_o.



Apply KVL to V_e node

$$\frac{V_{\pi 1}}{r_\pi} + g_m V_{\pi 1} + g_m V_{\pi 2} + \frac{V_{\pi 2}}{r_\pi} - \frac{V_e}{R_E} = 0 \quad \text{—①}$$

$$\frac{V_{\pi 1} + g_m V_{\pi 1} r_\pi}{r_\pi} + \frac{g_m V_{\pi 2} r_\pi + V_{\pi 2}}{r_\pi} = \frac{V_e}{R_E} \quad \text{—②}$$

Sub $g_m r_\pi = \beta$ in ②

$$\frac{V_{\pi 1} + \beta V_{\pi 1}}{r_\pi} + \frac{\beta V_{\pi 2} + V_{\pi 2}}{r_\pi} = \frac{V_e}{R_E}$$

$$V_{\pi 1}\frac{(1+\beta)}{r_\pi} + V_{\pi 2}\frac{(1+\beta)}{r_\pi} = \frac{V_e}{R_E} \quad \text{—③}$$

From the ckt

$$\frac{V_{\pi 1}}{r_\pi} = \frac{V_{b1} - V_e}{r_\pi + R_B} \quad \text{and} \quad \frac{V_{\pi 2}}{r_\pi} = \frac{V_{b2} - V_e}{r_\pi + R_B}$$

$$V_{\pi 1} = \frac{r_\pi (V_{b1} - V_e)}{r_\pi + R_B} \quad \text{and} \quad V_{\pi 2} = \frac{r_\pi (V_{b2} - V_e)}{r_\pi + R_B} \quad \text{— (4)}$$

Sub values of $V_{\pi 1}$ & $V_{\pi 2}$ from (4) in (3)

$$\frac{r_\pi (V_{b1} - V_e)}{r_\pi + R_B}\left(\frac{1+\beta}{r_\pi}\right) + \frac{r_\pi (V_{b2} - V_e)}{r_\pi + R_B}\left(\frac{1+\beta}{r_\pi}\right) = \frac{V_e}{R_E}$$

$$\frac{V_{b1} + V_{b2} - 2V_e}{r_\pi + R_B}(1+\beta) = \frac{V_e}{R_E}$$

Solving for V_e

$$\frac{V_{b1} + V_{b2} - 2V_e}{r_\pi + R_B} = \frac{V_e}{R_E(1+\beta)}$$

$$\frac{V_{b1} + V_{b2}}{r_\pi + R_B} = \frac{V_e}{R_E(1+\beta)} + \frac{2V_e}{r_\pi + R_B}$$

$$\frac{V_{b1} + V_{b2}}{r_\pi + R_B} = \frac{V_e r_\pi + R_B V_e + 2V_e R_E + 2V_e R_E \beta}{R_E(1+\beta)(r_\pi + R_B)}$$

$$\frac{V_{b1} + V_{b2}}{r_\pi + R_B} = \frac{V_e (r_\pi + R_B) + 2V_e R_E (1+\beta)}{R_E(1+\beta)(r_\pi + R_B)}$$

$$= \frac{V_e\left[(r_\pi + R_B) + 2R_E(1+\beta)\right]}{R_E(1+\beta)(r_\pi + R_B)}$$

$$V_e = \frac{V_{b1} + V_{b2}}{(r_\pi + R_B) + 2R_E(1+\beta)} \times R_E(1+\beta)$$

$$V_e = \frac{V_{b1} + V_{b2}}{2 + \frac{r_\pi + R_B}{R_E(1+\beta)}} \quad \text{— (5)}$$

One sided o/p at collector of Q_2 is given by

$$V_o = V_{C_2} = -(g_m V_{\pi_2}) R_C = -g_m r_\pi \left(\frac{V_{\pi_2}}{r_\pi}\right) R_C \quad \text{— (6)}$$

Sub V_{π_2}/r_π from (4) in (6)

$$V_o = -g_m r_\pi \left(\frac{V_{b_2} - V_e}{r_\pi + R_B}\right) R_C = -\beta R_C \left(\frac{V_{b_2} - V_e}{r_\pi + R_B}\right) \quad \because g_m r_\pi = \beta \quad \text{— (7)}$$

Sub (5) in (7)

$$V_o = -\beta R_C \left[\frac{V_{b_2} - \dfrac{(V_{b_1} + V_{b_2})}{2 + \dfrac{r_\pi + R_B}{(1+\beta) R_E}}}{r_\pi + R_B}\right]$$

$$V_o = \frac{-\beta R_C}{r_\pi + R_B} \left[\frac{2V_{b_2} + V_{b_2}\left(\dfrac{r_\pi + R_B}{(1+\beta) R_E}\right) - V_{b_1} + V_{b_2}}{2 + \dfrac{r_\pi + R_B}{(1+\beta) R_E}}\right]$$

$$= \frac{-\beta R_C}{r_\pi + R_B} \cdot \frac{V_{b_2}\left(1 + \dfrac{r_\pi + R_B}{(1+\beta) R_E}\right) - V_{b_1}}{2 + \dfrac{r_\pi + R_B}{(1+\beta) R_E}} \quad \text{— (8)}$$

For ideal current source $R_E = \infty$

$$V_o = \frac{-\beta R_C (V_{b_2} - V_{b_1})}{2(r_\pi + R_B)} \quad \text{— (9)}$$

$$V_o = \frac{\beta R_c}{2(r_\pi + R_B)} \cdot V_d + \frac{\left(V_{cm} - \frac{V_d}{2}\right)\left(\frac{r_\pi + R_B}{(1+\beta) R_E}\right)}{2 + \frac{r_\pi + R_B}{(1+\beta) R_E}}$$

$$V_o = \frac{\beta R_c}{2(r_\pi + R_B)} \cdot V_d - \frac{g_m R_c}{1 + \frac{2(1+\beta) R_E}{r_\pi + R_B}} \cdot V_{cm} \quad \text{— (1)}$$

$$V_o = A_d V_d + A_{cm} V_{cm} \quad \text{— (2)}$$

comparing (1) & (2)

$$A_d = \frac{\beta R_c}{2(r_\pi + R_B)} \quad \text{and} \quad A_{cm} = \frac{-g_m R_c}{1 + \frac{2(1+\beta) R_o}{r_\pi + R_B}}$$

Considering Source resistors $R_B = 0$;

$$A_d = \frac{\beta R_c}{2 r_\pi} = \frac{g_m R_c}{2} = \frac{I_{CQ} R_c}{2 V_T}$$

$\because g_m = \frac{\beta}{r_\pi}$ & $g_m = \frac{I_{CQ}}{V_T}$

$$A_d = \frac{I_Q R_c}{4 V_T}$$

$$I_{CQ} = \frac{I_Q}{2}$$

$$A_{cm} = \frac{-g_m R_c}{1 + \frac{2(1+\beta) R_o}{r_\pi}} = \frac{-\frac{I_{CQ} R_c}{V_T}}{1 + \frac{2(1+\beta) R_o g_m}{\beta}}$$

$$r_\pi = \frac{\beta}{g_m}$$

$$= \frac{-\frac{I_{CQ} R_c}{V_T}}{\frac{1 + 2(1+\beta) R_E I_{CQ}}{V_T \beta}} = \frac{-\frac{I_Q R_c}{2 V_T}}{1 + \frac{2(1+\beta) R_E I_Q}{2 V_T \beta}}$$

$$CMRR = \rho = \frac{A_d}{A_{CM}}$$

$$= \frac{\frac{I_{CQ} R_c}{2 V_T}}{\frac{I_{CQ} R_c}{\frac{V_T}{1 + (1+\beta) R_E I_Q}{V_T \beta}}} = \frac{1}{2}\left[1 + \frac{(1+\beta) R_E I_Q}{V_T \beta}\right]$$

$$A_d = \frac{V_o}{V_d} = \frac{-\beta R_c (V_{b_2} - V_{b_1})}{2 V_d (r_\pi + R_B)}$$

$$A_d = \frac{\beta R_c}{2(r_\pi + R_B)} \qquad \left[\because V_d = (V_{b_1} - V_{b_2}),\ V_{b_2} - V_{b_1} = -V_d\right]$$

If $R_B = 0$

$$A_d = \frac{\beta R_c}{2 r_\pi} = \frac{g_m r_\pi R_c}{2 r_\pi} \qquad \left[\because g_m r_\pi = \beta\right]$$

$$\boxed{A_d = \frac{g_m R_c}{2}}$$

is identical to voltage transfer characteristics

$$V_{b_1} = V_{cm} + \frac{V_d}{2} \quad ; \quad V_{b_2} = V_{cm} - \frac{V_d}{2} \qquad \text{---(10)}$$

[V_{cm} - common mode voltage]

Sub (10) in (8)

$$V_o = -\beta R_c \left[\frac{\left(V_{cm} - \frac{V_d}{2}\right)\left[1 + \frac{r_\pi + R_B}{(1+\beta) R_E}\right] - \left(V_{cm} + \frac{V_d}{2}\right)}{2 + \frac{r_\pi + R_B}{(1+\beta) R_o}} \right] \qquad \text{---(11)}$$

Unit - IV

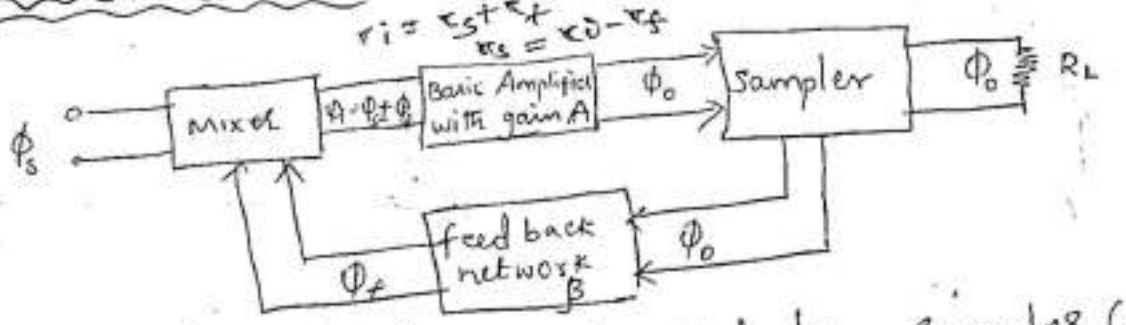
Feedback Amplifiers

Concepts

* In large signal amplifiers and measuring instruments distortion should be avoided.
* gain must be independent of variation in voltage of dc supply, and values of circuit components.
* This is achieved by feedback, portion of output signal is combined with normal input signal and feedback is accomplished.

GAIN WITH FEED BACK

BLOCK DIAGRAM!



* output quantity is sampled by sampler (voltage, current) and fed to the feedback network.
* output of feedback network is combined with external source signal ϕ_s throu' mixer and fed to basic amplifier.
* mixer is of two types series mixer and shunt mixer.

$$A - \text{gain} = \frac{\phi_o}{\phi_i}$$

$$\beta - = \frac{\phi_f}{\phi_o}$$

A_f - gain of feedback Amplifier $= \frac{\phi_o}{\phi_s}$

ϕ_s - a.c signal in the input side

ϕ_f - feedback signal

Positive feedback

* If the feedback signal ϕ_f is in phase with i/p signal ϕ_s, the net effect will increase the input signal. $\phi_i = \phi_s + \phi_f$.

* The input voltage applied to basic amplifier is increased by increasing ϕ_o exponentially.

* This type of feedback is positive or regenerative feedback.

* Gain of the amplifier is,

$$A_f = \frac{\phi_o}{\phi_s} = \frac{\phi_o}{\phi_i - \phi_f} = \frac{1}{\frac{\phi_i}{\phi_o} - \frac{\phi_f}{\phi_o}} = \frac{1}{\frac{1}{A} - \beta} = \frac{A}{1 - A\beta}$$

$|A_f| > |A|$. loop gain $= A\beta$

* product of open loop gain and feed back factor is called loop gain.

* If $|A\beta| = 1$, then $A_f = \infty$. the gain of amplifier with positive feedback is infinite and amplifier gives a.c o/p without ac i/p. and acts as an oscillator.

* +ve fdb. increases instability and reduces the bandwidth and increases distortion and noise

Negative feedback

* If the feedback ϕ_f is out of phase with input signal then $\phi_i = \phi_s - \phi_f$.

* The input voltage is decreased and the output is decreased

* Voltage gain is reduced and feedback is negative or degenerative feedback.

* Gain of amplifier with negative feedback

$$A_f = \frac{\phi_o}{\phi_s} = \frac{\phi_o}{\phi_i + \phi_f} = \frac{1}{\frac{\phi_i}{\phi_o} + \frac{\phi_f}{\phi_o}} = \frac{1}{\frac{1}{A} + \beta}$$

$$A_f = \frac{A}{1+\beta A},$$

* $|A_f| < |A|$. If $|A\beta| \gg 1$. $A_f = 1/\beta$,

β is feedback ratio.

* -ve feedback improves the performance of electronic amplifiers.

* -ve feedback increase bandwidth, decrease distortion and noise

Effects of negative feedback on gain stability

Gain $A_f = \frac{A}{1+A\beta}$ $\quad \frac{dA_f}{dA} = \frac{vu' - uv'}{v^2}$

Diff. w.r.to A

$$\frac{dA_f}{dA} = \frac{1}{(1+A\beta)^2} = \frac{A_f}{A}\frac{1}{1+A\beta}$$

* $\therefore \quad \frac{dA_f}{A_f} = \frac{dA}{A} \quad \frac{1}{1+A\beta}$

* $\frac{dA_f}{A_f}$ represents fractional change in amp Volt. gain with feedback

* $\frac{dA}{A}$ denotes fractional change in Voltage gain without feedback.

* $\frac{1}{1+A\beta}$ is called sensitivity.

* Sensitivity is defined as ratio of % change in voltage gain without feedback

$$\text{Sensitivity} = \frac{\left(\frac{dA_f}{A_f}\right)}{\left(\frac{dA}{A}\right)} = \frac{1}{1+A\beta}$$

* reciprocal of the term Sensitivity is called desensitivity.

$$\text{desensitivity} = 1+A\beta$$

Cutoff Frequencies:

* Bandwidth of an amplifier is the difference between the upper cutoff f_2 and lower cutoff frequency f_1.

* The product of Voltage gain and B.W of an amplifier without feedback and with feedback remains the same (ie) $A_f \times BW_f = A \times BW$

* Decreased Noise

* many sources of noise depending upon active devices
* Using negative feedback with feedback ratio β, the noise N, can be reduced by factor $\frac{1}{1+A\beta}$
* The noise with feedback is given by

$$N_f = \frac{N}{1+A\beta}$$

Increased in Input Impedance:

* Amplifier should have high input impedance, so that it will not load the preceding stage
* It is achieved by negative series voltage feedback
* Input impedance with feedback is given by

$$Z_{if} = Z_i (1+A\beta)$$

Decrease in Output Impedance

* amplifier with low o/p impedance is capable of delivering power to load without loss
* It is achieved by negative series voltage feedback in an amplifier
* The output impedance is

$$Z_{of} = \frac{Z_o}{1+A\beta}$$

* output impedance is reduced by factor $1+A\beta$

* The Voltage gain of feedback amplifier reduces by the factor $1/1+A\beta$

* Bandwidth is increased by $1+A\beta$.

$$BW_f = BW(1+A\beta)$$

$A \rightarrow$ midband gain without feedback.

* Due to negative feedback upper cutoff frequency f_{2f} is increased by factor $(1+A\beta)$.

* lower cutoff freq f_{1f} is decreased by factor $(1+A\beta)$.

* upper and lower 3dB freq. with negative feedback is given by

$$f_{2f} = f_2(1+A\beta) \quad \text{and} \quad f_{1f} = \frac{f_1}{(1+A\beta)}$$

Decreased Distortion

* An amplifier with an open loop Voltage gain and a total harmonic distortion D,

* The introduction of negative feedback with feedback ratio β, the distortion will reduce to

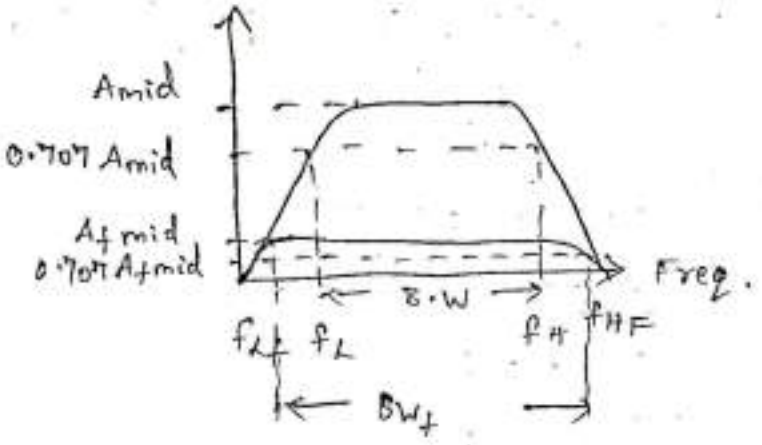
$$D_f = \frac{D}{1+A\beta}$$

Bandwidth

BW = Upper cutoff frequency − Lower cut off freq.

$$BW_f = f_{Hf} - f_{Lf} = (1 + A_{mid}\beta) f_H - \frac{f_L}{1 + A_{mid}\beta}$$

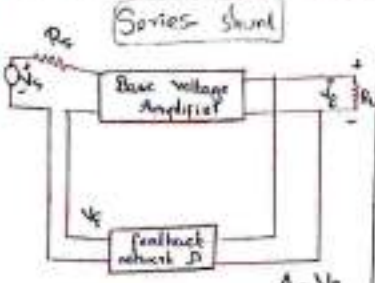
* $(f_{Hf} - f_{Lf}) > (f_H - f_L)$ ∴ hence B.W of amplifier with feedback is greater than B.W of amplifier without feedback



Voltage Series

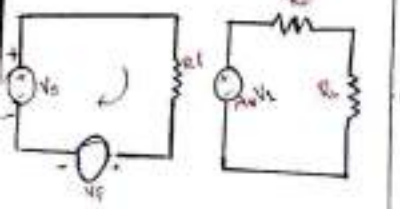
(voltage mixing voltage sampling)

(Series - Shunt)



$A = \frac{V_o}{V_f}$

Input Impedance :-



Apply KVL to input circuit

$V_s - I_i R_i - V_f = 0$ $\quad A_v = \frac{V_o}{V_i}$

$V_s = I_i R_i + V_f$ $\quad A_v\beta = 1$, $\beta = \frac{V_f}{V_o}$

$= I_i R_i + \beta V_o \rightarrow (1)$ $\quad R = \frac{V_i}{I_i}$

$V_o = A_v V_i \left(\frac{R_o}{R_o + R_o}\right) = A_f V_i$

$\Rightarrow A_{vf} I_i R_i \rightarrow (2)$ $\quad A_{vf} = \frac{V_o}{V_f}$

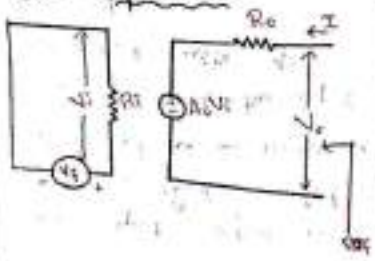
Subs (2) in (1).

$V_s = I_i R_i + \beta A_{vf} I_i R_i$

$V_s = I_i R_i (1 + \beta A_{vf})$

$$R_{if} = \frac{V_s}{I_i} = R_i (1 + \beta A_{vf})$$

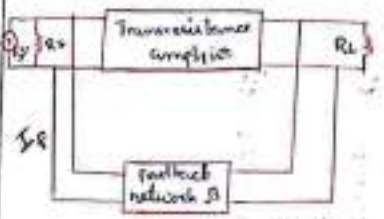
Output Impedance



Voltage Shunt

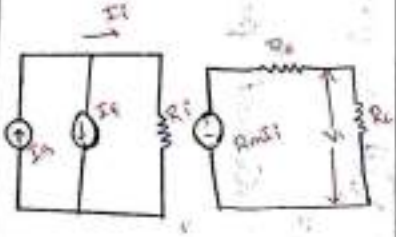
(current mixing voltage sampling)

(Shunt - Shunt)



$A = \frac{V_o}{I_f}$

Input Impedance



Darlington

$R_m = \frac{V_o}{I_i}$

$V_o = R_m I_i$

Apply KCL at input node,

$I_f = \beta V_o$

$I_s = I_i + I_f$

$= I_i + \beta V_o \rightarrow (1)$

The output voltage V_o is given by,

$V_o = R_m I_i \times \frac{R_L}{R_L + R_o}$

$= R_{mf} I_i \rightarrow (2)$

Subs (2) in (1)

$I_s = I_i + \beta R_{mf} I_i$

$I_s = I_i (1 + \beta R_{mf})$

Input resistance with feedback is R_{if}.

$R_{mf} = \frac{R_m R_L}{R_L + R_o}$

$R_{if} = \frac{V_i}{I_s}$

$R_{if} = \frac{V_i}{I_i (1 + \beta R_{mf})}$

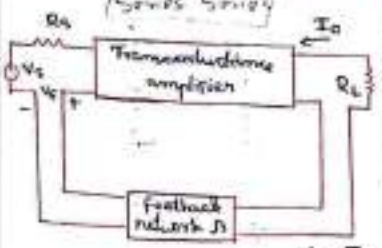
$$R_{if} = \frac{R_i}{1 + \beta R_{mf}}$$

$R_i = \frac{V_i}{I_i}$

Current series

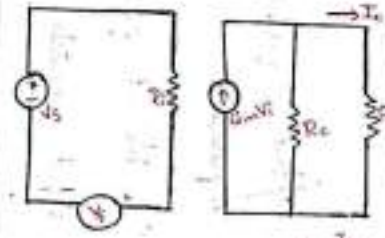
(voltage mixing current sampling)

(Series - Series)



$A = \frac{I_o}{V_f}$

Input Impedance



$G = \frac{I_o}{V_i}$ $\quad \beta = \frac{V_f}{I_o}$

Apply KVL to input side

$V_s - I_i R_i - V_f = 0$

$V_s = I_i R_i + V_f$

$= I_i R_i + \beta I_o \rightarrow (1)$

From output circuit,

$I_o = G_m V_i \left(\frac{R_o}{R_o + R_L}\right)$

$= G_{mf} V_i \rightarrow (2)$ $\quad G_{mf} = \frac{G_m R_o}{R_o + R_L}$

Subs (2) in (1),

$V_s = I_i R_i + \beta G_{mf} V_i$

$= I_i R_i + \beta G_{mf} I_i R_i$

$= I_i R_i (1 + \beta G_{mf})$

$R_{if} = \frac{V_s}{I_i}$

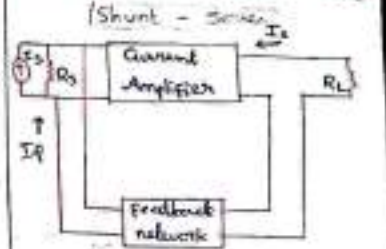
$= R_i (1 + \beta G_{mf})$

$$R_{if} = R_i (1 + \beta G_{mf})$$

Current Shunt

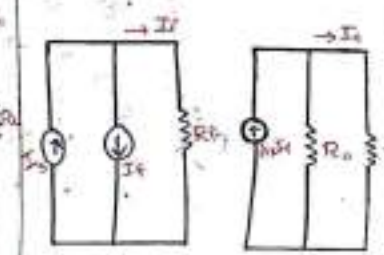
(current mixing current sampling)

(Shunt - Series)



$A = \frac{I_o}{I_f}$

Input Impedance :



$A_I = \frac{I_o}{I_i}$

$I_o = A_I I_i$

Apply KCL to input side,

$I_s = I_i + I_f$

$I_s = I_i + \beta I_o \rightarrow (1)$

$I_o = \frac{A_I I_i R_o}{R_o + R_L}$

$I_o = A_{If} I_i \rightarrow (2)$

$\therefore A_{If} = \frac{A_I R_o}{R_o + R_L}$

Subs (2) in (1),

$I_s = I_i + \beta A_{If} I_i$

$I_s = I_i (1 + \beta A_{If})$

$R_{if} = \frac{V_i}{I_s}$

$= \frac{V_i}{I_i (1 + \beta A_{If})}$

$R_i = \frac{V_i}{I_i}$

$$R_{if} = \frac{R_i}{(1 + \beta A_{If})}$$

For output impedance, input is shed circuited and resistance is measured by looking into the input from output with R_L disconnected.

Apply KVL to output side,

$A_v V_i + I R_o - V_o = 0$ $\quad \beta = \frac{V_f}{V_o}$, $V_f = \beta V_o$

$\therefore I = \frac{V_o - A_v V_i}{R_o} \rightarrow (1)$

$V_i = -V_f = -\beta V_o \rightarrow (2)$

Subs (2) in (1)

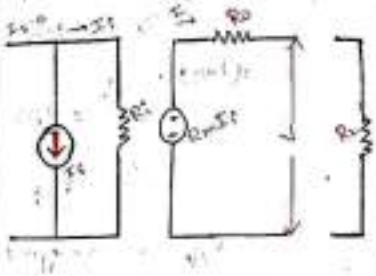
$I = \frac{V_o + A_v \beta V_o}{R_o}$

$I = \frac{V_o (1 + A_v \beta)}{R_o}$

$R_{of} = \frac{V}{I} = \frac{R_o}{1 + A_v \beta}$

This is the output impedance.

Output Impedance :



Apply KVL to output side

$R_m I_f + I R_o - V = 0$

$I = \frac{V - R_m I_f}{R_o} \rightarrow (1)$

$I_f = -I_f = -\beta V \rightarrow (2)$

Subs (2) in (1)

$I = \frac{V + R_m \beta V}{R_o}$

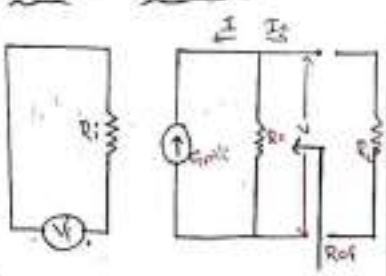
$I = \frac{V (1 + \beta R_m)}{R_o}$

Similarly,

$R_{of} = \frac{V}{I} = \frac{R_o}{1 + \beta R_m}$

This is the output impedance.

Output Impedance



Apply KCL to output circuit

$I = \frac{V}{R_o} - G_m V_i \rightarrow (1)$

Input voltage,

$V_i = -V_f$

$= -\beta I_o$

$= \beta I \rightarrow (2)$

Subs (2) in (1)

$I = \frac{V}{R_o} - G_m \beta I$

$\frac{V}{R_o} = I + G_m \beta I$

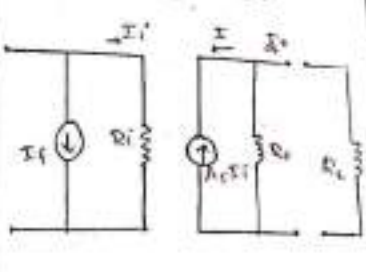
$\frac{V}{R_o} = I (1 + G_m \beta)$

$R_{of} \cdot \frac{V}{I} = R_o (1 + G_m \beta)$

$R_{of} = R_o (1 + G_m \beta)$

This is the output impedance.

Output Impedance



$I = \frac{V}{R_o} - A_I I_i \rightarrow (1)$

Input current,

$I_i = -\beta I_o$

$I_i = \beta I \rightarrow (2)$

Subs (2) in (1)

$I = \frac{V}{R_o} - A_I \beta I$

$\frac{V}{R_o} = I + A_I \beta I$

$= I (1 + A_I \beta)$

$\frac{V}{I} = R_o (1 + \beta A_I)$

$R_{of} = \frac{V}{I} = R_o (1 + \beta A_I)$

$R_{of} = R_o (1 + \beta A_I)$

This is the output impedance.

MUST STUDY

Unit - IV Oscillators

Concepts

→ The circuit which is used to generate periodic voltage without a.c input signal is called an oscillator

→ The circuit is supplied with energy from a d.c source

→ If the output is sine wave function of time the oscillator is called sinusoidal or harmonic oscillator

Classification of Oscillators

① According to wave form

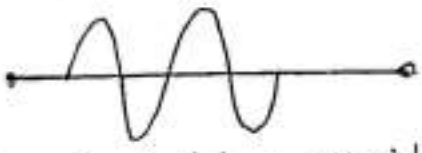
i) Sinusoidal oscillator

ii) Relaxation oscillator

Sinusoidal oscillator - generates sinusoidal voltages or current

Relaxation oscillator - generates voltage or current which vary abruptly one or more times in a cycle of oscillation

Wave form sinsoidal



Waveform for relaxation oscillator

② According to fundamental mechanism

i) negative resistance oscillator uses negative resistance of amplifying device to neutralize positive resistance of oscillation

ii) Feedback oscillator → uses positive feedback in feedback amplifier to satisfy Barkhausen criterion

③. According to frequency generated

i) Audio Frequency Oscillator – upto 20 KHz

ii) Radio Frequency oscillator – 20 KHz to 30 MHz

iii) VHF – 30 MHz to 300 MHz – Very High frequency

iv) UHF – 300 MHz to 3 GHz – Ultra High frequency

v) Microwave frequency – above 3 GHz

④ According to type of circuit used

a) LC tuned oscillator b) RC phase shift oscillator

Barkhausen criterion

→ The oscillator circuit is set to oscillation by random variation caused in base current due to noise component

→ The noise components (small random electrical voltages and currents are present in any conductor, tube or transistor

→ Even when no external signal is applied, noise will cause some signal at output of amplifier

→ amplifier tuned at particular frequency the output signal caused by noise is predominant at f_0.

→ If amplifier has gain of more 1/p, output increases and feedback signal becomes larger and goes on increasing

→ As signal level increases, gain decreases

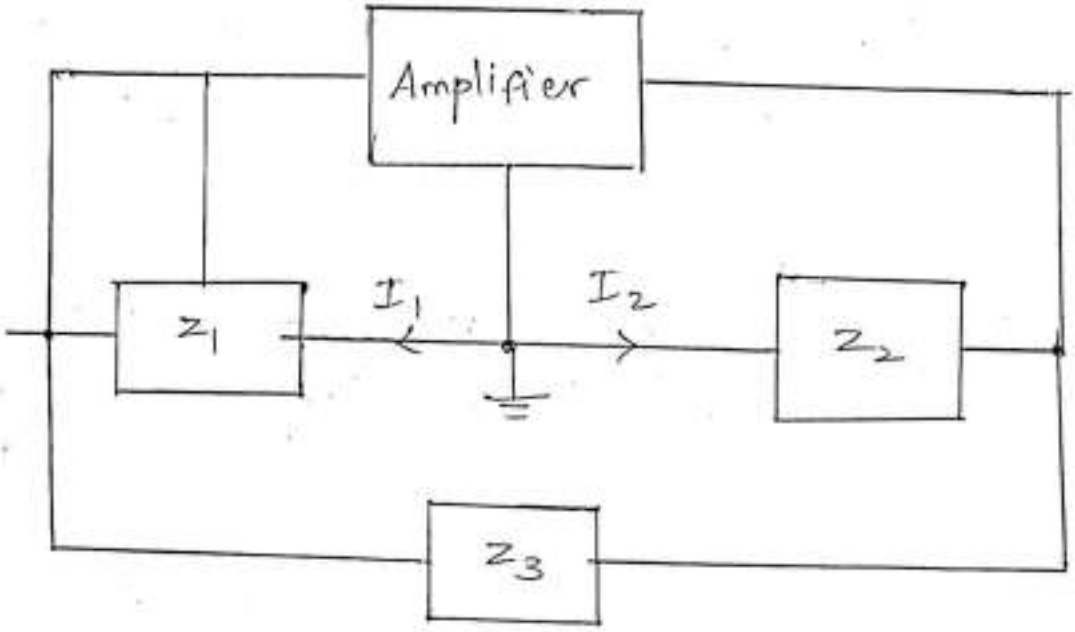
→ The gain is decreased at particular value of output. gain

→ The output voltage remains constant at f_0 called (frequency of oscillation)

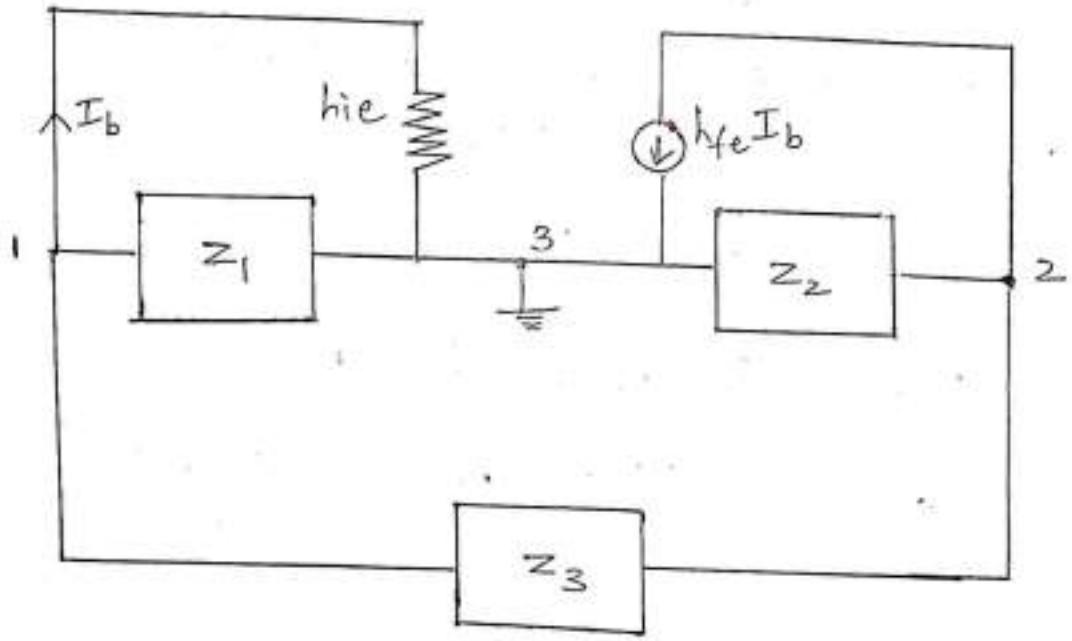
conditions for maintaining oscillation

1. $|A\beta| = 1$, loop gain must be unity
2. The total phase shift around closed loop is 0° or 360°

General form of an LC oscillator



Equivalent circuit



Z_1, Z_2, Z_3 → reactive elements inductor or capacitor of feedback tank circuit determines frequency of oscillation

Z_1, Z_2 → acts as voltage divider for output voltage and feedback signal

→ Voltage across Z_1 is feedback signal

Frequency of oscillation of LC oscillator is

$$f_o = \frac{1}{2\pi\sqrt{LC}}$$

Load impedance

Z_1 and hie are parallel.

→ Their equivalent impedance $Z' = Z_1 \parallel hie$

$$Z' = \frac{Z_1\, hie}{Z_1 + hie}$$

→ The load impedance Z_L between output terminals 2 and 3 is the impedance of Z_2 parallel with $Z' + Z_3$

$$\therefore Z_L = Z_2 \parallel Z' + Z_3 = \frac{Z_2(Z' + Z_3)}{Z_2 + Z' + Z_3} = \frac{Z_2 Z' + Z_2 Z_3}{Z_2 + Z' + Z_3}$$

$$= \frac{Z_2\left(\frac{Z_1\, hie}{Z_1 + hie}\right) + Z_2 Z_3}{Z_2 + \left(\frac{Z_1\, hie}{Z_1 + hie}\right) + Z_3} = \frac{Z_1 Z_2 hie + Z_1 Z_2 Z_3 + Z_2 Z_3 hie}{Z_2 Z_1 + Z_2 hie + Z_1 Z_3 + Z_3 hie + Z_1 hie}$$

$$= \frac{hie\,(Z_1 * Z_2 + Z_2 Z_3) + Z_1 Z_2 Z_3}{hie\,(Z_1 + Z_2 + Z_3) + Z_1 Z_2 + Z_1 Z_3} = \frac{hie\, Z_2\left[(Z_1 + Z_3) + Z_1 Z_3\right]}{hie(Z_1 + Z_2 + Z_3) + Z_1 Z_2 + Z_1 Z_3}$$

Voltage gain without feed back

$$A_{ve} = \frac{-h_{fe} Z_L}{hie}$$

Feed back fraction β

Output voltage in terms of current I_1 between terminals 3 & 1

$$V_o = -I_1 (Z' + Z_3) = -I_1 \left(\frac{Z_1 hie}{Z_1 + hie} + Z_3 \right)$$

$$= -I_1 \left(\frac{hie(Z_1 + Z_3) + Z_1 Z_3}{Z_1 + hie} \right)$$

Voltage feedback to input terminals 3 & 1 is given by

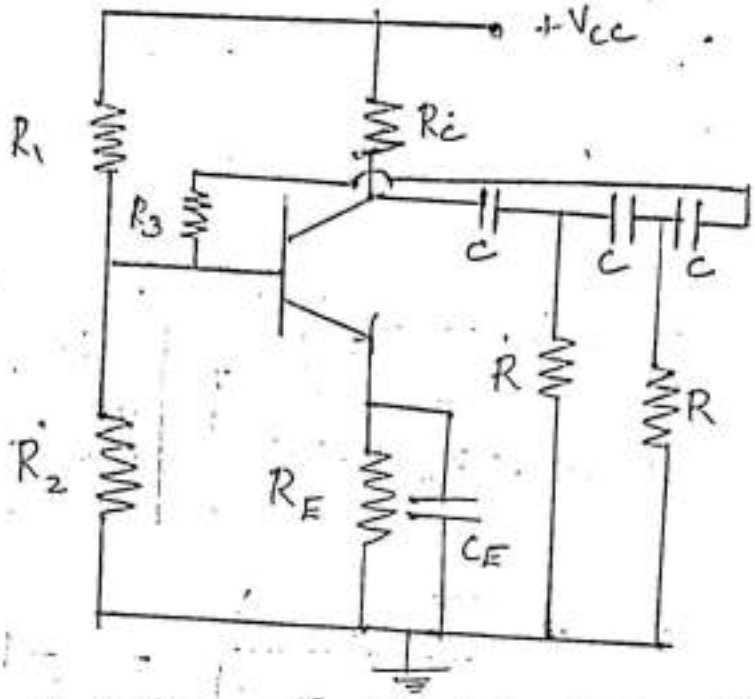
$$V_{fb} = -I_1 Z' = I_1 \left(\frac{Z_1 hie}{Z_1 + hie} \right)$$

$$\beta = \frac{V_{fb}}{V_o} = I_1 \left(\frac{Z_1 hie}{Z_1 + hie} \right) \left(\frac{Z_1 + hie}{hie(Z_1 + Z_3) + Z_1 Z_3} \right) I_1$$

$$\beta = \frac{Z_1 hie}{hie(Z_1 + Z_3) + Z_1 Z_3}$$

RC - Phase shift Oscillator

→ RC oscillator operate at low frequency



→ Common Emitter amplifier is followed by 3 RC section
→ The output of the last Rc network is fed to input
→ To make 3 RC sections identical, R_3 is chosen as $R_3 = R - R_i$

R_i — input impedance

→ Phase shift is $\phi = \tan^{-1}\left(\frac{1}{\omega CR}\right)$

→ The Resistor 'R' is adjusted to give $\phi = 60°$

→ For a given frequency fo the RC ladder network produces a total phase shift of 180° between input and output

→ The total phase shift from base of transistor around circuit to base is 360°

Equation for oscillation

$$A_{ve}\beta = 1$$

$$\left(\frac{-h_{fe} z_1}{h_{ie}}\right)\left[\frac{z_1 h_{ie}}{h_{ie}(z_1+z_3)+z_1 z_3}\right] = 1$$

$$\left\{\frac{h_{fe} z_2 \left[\cancel{h_{ie}(z_1+z_3)+z_1 z_3}\right]}{h_{ie}(z_1+z_2+z_3)+z_1 z_2+z_1 z_3}\right\}\left[\frac{z_1}{\cancel{h_{ie}(z_1+z_3)+z_1 z_3}}\right] = -1$$

$$\left(\frac{h_{fe} z_2 z_1}{h_{ie}(z_1+z_2+z_3)+z_1 z_2+z_1 z_3}\right) = -1$$

$$h_{ie}(z_1+z_2+z_3)+z_1 z_2+z_1 z_3 = -h_{fe} z_1 z_2$$

$$\boxed{h_{ie}(z_1+z_2+z_3)+z_1 z_2(1+h_{fe})+z_1 z_3 = 0}$$

is the general equation for oscillator

The frequency of oscillation

$$f_0 = \frac{1}{2\pi RC\sqrt{6}}$$

→ At this frequency the feedback factor $|\beta| = 1/29$

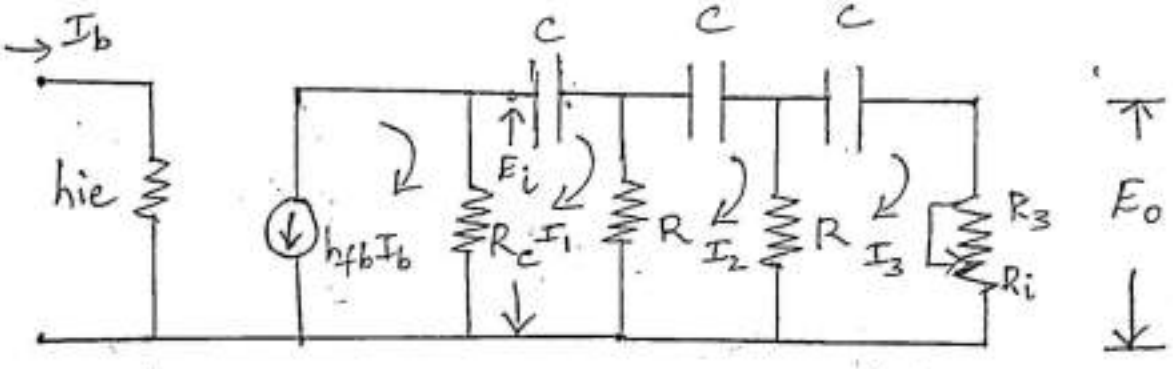
$A\beta > 1$, $|A| > 29$ for operation

→ It is suitable for audio frequency only

Draw back

1. the 3 RC network must be changed simultaneously to change frequency.
2. It is difficult to control amplitude of oscillation without affecting frequency of oscillation.

Analysis



From the fig.

loop1 : $R(I_1 - I_2) + \frac{I_1}{j\omega C} = E_i$

$$I_1\left(R + \frac{1}{j\omega C}\right) - I_2 R = E_i$$

loop 2: $R(I_2 - I_1) + \frac{I_2}{jwC} + R(I_2 - I_3) = 0$

$$-I_1 R + I_2\left(2R + \frac{1}{jwC}\right) - I_3 R = 0$$

loop 3: $R(I_3 - I_2) + \frac{I_3}{jwC} + (R_3 + R_i) I_3 = 0$

$$-I_2 R + I_3\left(2R + \frac{1}{jwC}\right) = 0$$

Replacing jw by s & writing equation

$$\begin{bmatrix} R + \frac{1}{jwC} & -R & 0 \\ -R & 2R + \frac{1}{jwC} & -R \\ 0 & -R & 2R + \frac{1}{jwC} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} E_i \\ 0 \\ 0 \end{bmatrix}$$

Applying cramers rule

$$I_3 = \frac{\Delta_3}{\Delta} \quad \text{---} \quad (1)$$

$$\Delta_3 = \begin{bmatrix} R + \frac{1}{jwC} & -R & E_i \\ -R & 2R + \frac{1}{jwC} & 0 \\ 0 & -R & 0 \end{bmatrix} = E_i R^2 \quad \text{---} \quad (2)$$

$$\Delta = \begin{bmatrix} R+\frac{1}{jwc} & -R & 0 \\ -R & 2R+\frac{1}{jwc} & -R \\ 0 & -R & 2R+\frac{1}{jwc} \end{bmatrix}$$

$$= \left(R+\frac{1}{jwc}\right)\left[\left(2R+\frac{1}{jwc}\right)^2 - R^2\right] - R^2\left(2R+\frac{1}{jwc}\right)$$

$$= \frac{(jwcR+1)(2Rjwc+1)^2}{j^3w^3c^3} - \frac{R^2(jwcR+1)}{jwc} - \frac{\left[R^2(2jwcR+1)\right]}{jwc}$$

$$= \left[\frac{(jwcR+1)(-4R^2w^2c^2+1+4Rjwc)}{j^3w^3c^3}\right] - \left[\frac{jwcR^3+R^2+2jwcR^3+R^2}{jwc}\right]$$

$$= \left[\frac{-4jR^3w^3c^3 - 4R^2w^2c^2 + jwcR + 1 - 4R^2w^2c^2 + 4Rjwc}{j^3w^3c^3}\right] - \left[\frac{3jwcR^3+2R^2}{jwc}\right]$$

$$= \frac{-4jR^3w^3c^3 - 4R^2w^2c^2 + jwcR + 1 - 4R^2w^2c^2 + 4Rjwc + 3jwcR^3 - 2j^2R^2w^2c^2}{j^3w^3c^3}$$

$$= \frac{(-4jR^3w^3c^3 - 8R^2w^2c^2 + 5jwcR + 1 + 3jw^3c^3R^3 + 2R^2w^2c^2)}{j^3w^3c^3}$$

$$= (-jR^3w^3c^3 - 6R^2w^2c^2 + 5jwcR + 1) / j^3w^3c^3$$

$$= \left(R^3\omega^3C^3 - 6jR^2\omega^2C^2 - 5\omega CR + j\right) / \omega^3C^3$$

Replace ωCR by $1/\alpha$

$$= \left(\frac{1}{\alpha^3} - \frac{6j}{\alpha^2} - \frac{5}{\alpha} + j\right) / \left(\frac{1}{\alpha R}\right)^3$$

$$= \left(1 - 6j\alpha - 5\alpha^2 + j\alpha^3\right) / \left(1/R^3\right)$$

$$\Delta = R^3\left[\left(1 - 5\alpha^2\right) + j\alpha\left(\alpha^2 - 6\right)\right] \quad \text{—③}$$

Sub ② and ③ in ①

$$I_3 = \frac{E_i R^2}{R^3\left[\left(1 - 5\alpha^2\right) + j\alpha\left(\alpha^2 - 6\right)\right]}$$

$$I_3 = \frac{E_i}{R} \cdot \frac{1}{\left(1 - 5\alpha^2\right) + j\alpha\left(\alpha^2 - 6\right)}$$

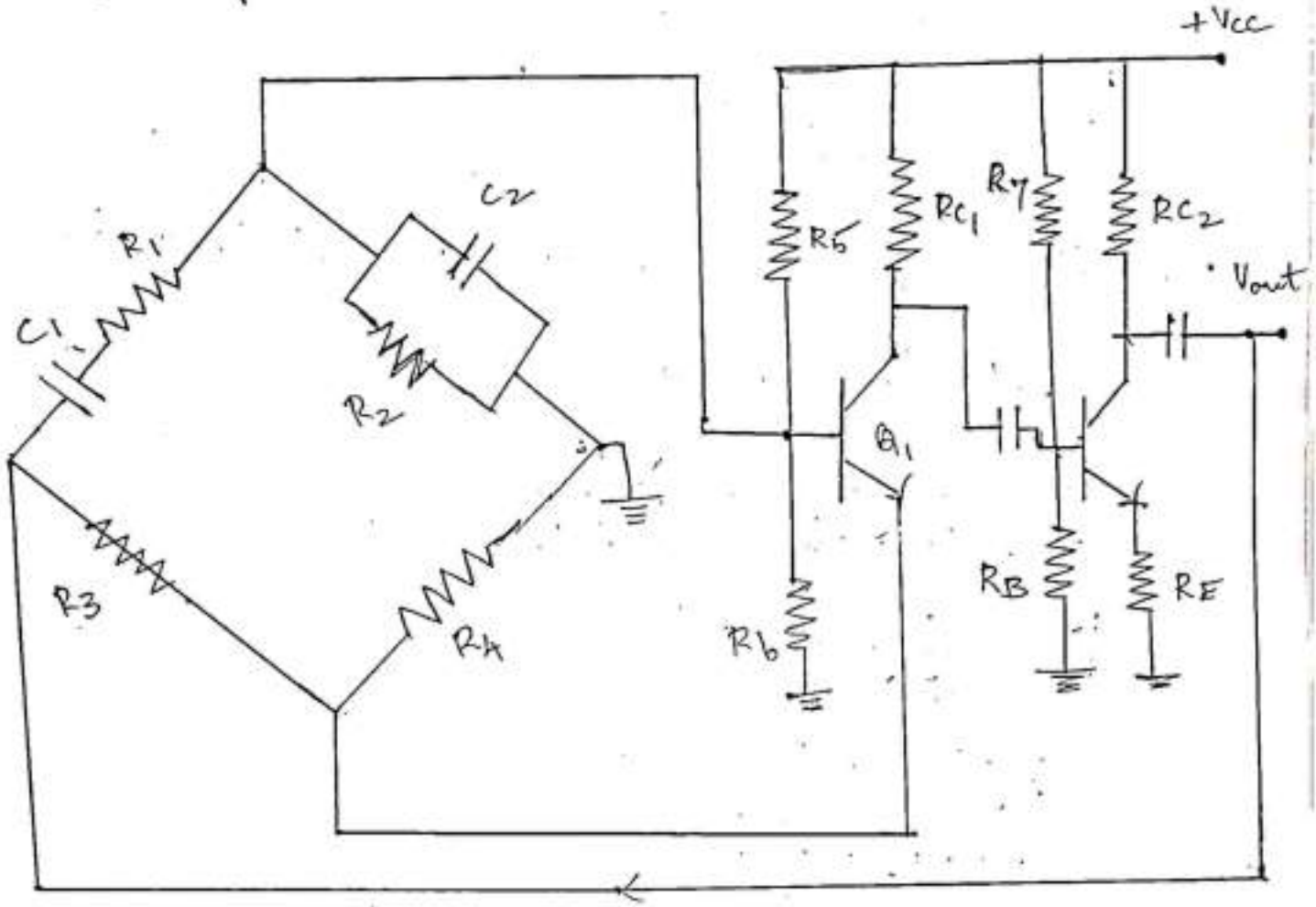
$$E_0 = I_3 R = E_i \times \frac{1}{\left(1 - 5\alpha^2\right) + j\alpha\left(\alpha^2 - 6\right)}$$

$$\beta = \frac{E_0}{E_i} = \frac{1}{1 - 5\alpha^2 + j\alpha\left(\alpha^2 - 6\right)} \quad \text{—④}$$

frequency of oscillation is determined by equating imaginary part to 0

$$\alpha\left(\alpha^2 - 6\right) = 0$$

Wein Bridge oscillator



→ Consists of two stage RC coupled amplifier provides phase shift of 360°

→ Balanced bridge is used as feedback network and provides no phase shift

→ The feedback network consists of lead-lag network R_1-C_1 and R_2-C_2 and voltage divider R_3-R_4

$$\alpha = \frac{1}{\omega_r CR} = \sqrt{6}$$

$$f_r = \frac{1}{2\pi RC\sqrt{6}}$$

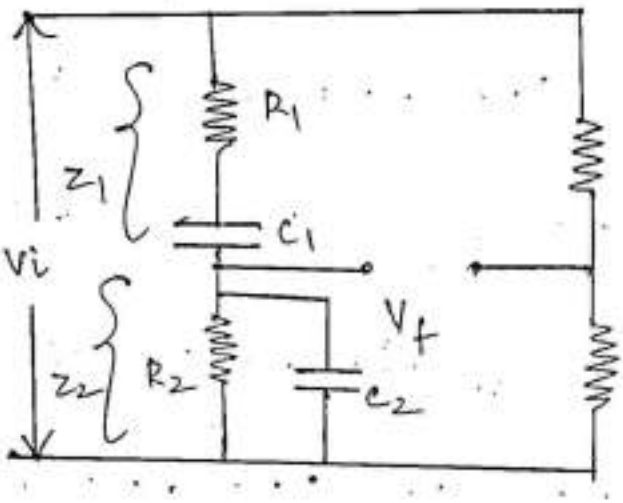
condition for oscillation is obtained by sub $\alpha = \sqrt{6}$ in (4)

$$\beta = \frac{1}{1-5\times 6} = \frac{-1}{29}$$

$$|\beta| = \frac{1}{29} \angle 180^\circ$$

$$|A\beta| = 1$$

$$\boxed{|A| > 29}$$



$V_f = V_1 - V_2$

$$V_1 = \frac{Z_2}{Z_1+Z_2} \times V_i \quad ; \quad V_2 = \frac{R_4}{R_3+R_4} \times V_i$$

$$V_f = \left[\left(\frac{Z_2}{Z_1+Z_2}\right) - \left(\frac{R_4}{R_3+R_4}\right)\right] V_i$$

$$Z_1 = R_1 + \frac{1}{jwC_1} = R_1 + \frac{1}{sC_1} = \frac{1+sC_1R_1}{sC_1}$$

$$Z_2 = R_2 \| \frac{1}{jwC_2} = R_2 \| \frac{1}{sC_2} = \frac{R_2 \times \frac{1}{sC_2}}{R_2 + \frac{1}{sC_2}} = \frac{R_2}{sC_2R_2+1}$$

$$\frac{Z_2}{Z_1+Z_2} = \frac{R_2/1+sC_2R_2}{\frac{1+sC_1R_1}{sC_1} + \frac{R_2}{sC_2R_2+1}} = \frac{R_2 \times sC_1}{(1+sC_2R_2)(1+sC_1R_1)+R_2sC_1}$$

$$= \frac{sC_1R_2}{1+sC_1R_1+sC_2R_2+s^2C_1C_2R_1R_2+R_2sC_1}$$

Sub $s = jw$

$$= \frac{jw\,C_1R_2}{(1-w^2C_1C_2R_1R_2)+jw(C_1R_1+C_2R_2+C_1R_2)}$$

$$= \frac{jwC_1R_2\left[1-w^2C_1C_2R_1R_2-jw(C_1R_1+C_2R_2+C_1R_2)\right]}{(1-w^2C_1C_2R_1R_2)^2+w^2(C_1R_1+C_2R_2+C_1R_2)^2}$$

$$= \frac{jwC_1R_2(1-w^2C_1C_2R_1R_2)+w^2(C_1R_1+C_2R_2+C_1R_2)}{(1-w^2C_1C_2R_1R_2)^2+w^2(C_1R_1+C_2R_2+C_1R_2)^2}$$

$$V_f = \left[\frac{w^2(C_1R_1+C_2R_2+C_1R_2)}{(1-w^2C_1C_2R_1R_2)^2+w^2(C_1R_1+C_2R_2+C_1R_2)^2} + \frac{jwC_1R_2(1-w^2C_1C_2R_1R_2)}{(1-w^2C_1C_2R_1R_2)^2+w^2(C_1R_1+C_2R_2+C_1R_2)^2} - \frac{R_3}{R_3+R_4}\right]V_i$$

Equating imaginary part to 0

$$jwCR_2(1-w^2C_1C_2R_1R_2)=0$$

$$w^2C_1C_2R_1R_2=1$$

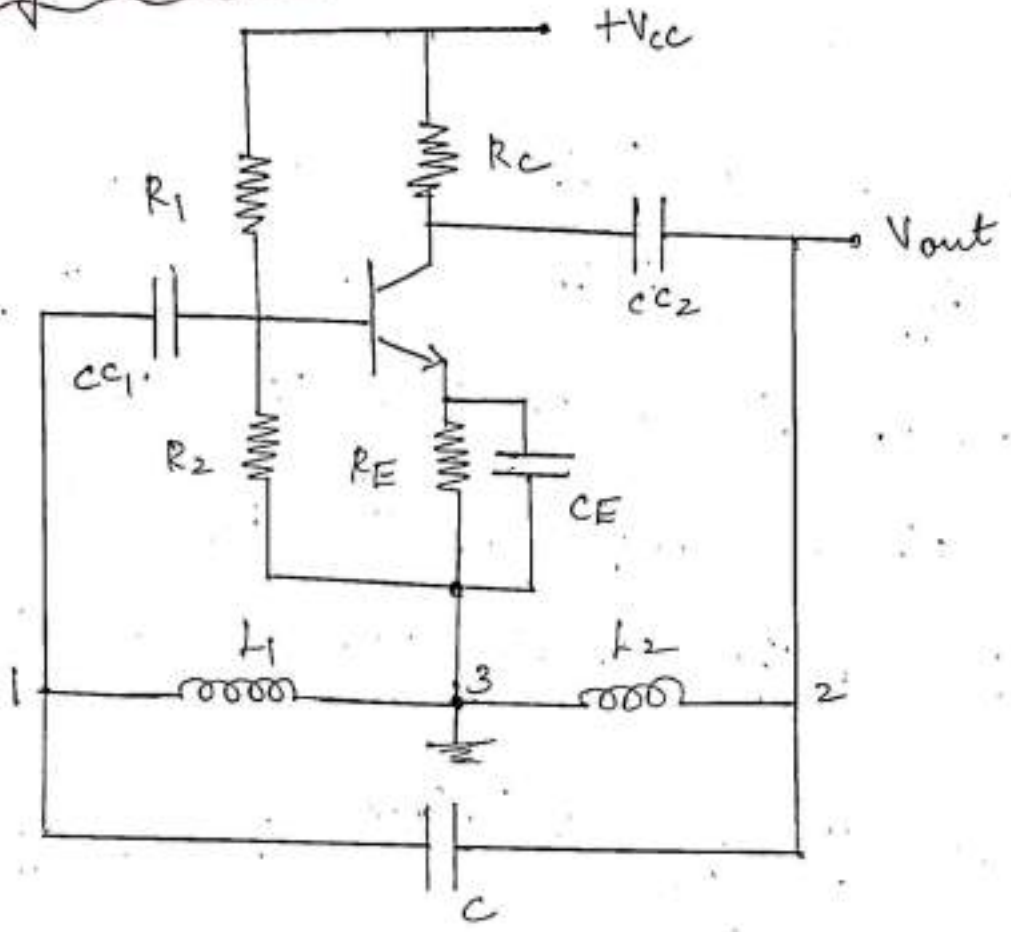
$$w=\frac{1}{\sqrt{C_1C_2R_1R_2}}$$

$$f_r=\frac{1}{2\pi\sqrt{C_1C_2R_1R_2}}$$

$$\boxed{f_r=\frac{1}{2\pi RC}} \qquad \left[\because\ R=R_1=R_2,\ C=C_1=C_2\right]$$

$R_3/R_4 > 2$ → provide sufficient gain for the circuit to osillate at desired frequency

Hartley Oscillator



→ Z_1, Z_2 → inductors, Z_3 → capacitor

→ R_1, R_2 and R_E → provides dc bias to transistor

→ C_E is bypass capacitor

→ CC_1, CC_2 are coupling capacitor

→ The feedback network consists of L_1, L_2 and C which determines the frequency of oscillator

→ when V_{cc} is ON transient current is produced in tank circuit and damped harmonic oscillation are set up in circuit

→ oscillatory current in tank circuit produces ac voltages across L_1 and L_2

→ If 3 is ground, 1 is +ve, 2 is -ve

→ Phase difference between 1 & 2 is always 180°

→ In CE, transistor provides 180° phase shift

→ Total phase shift is 180° + 180° = 360°

→ If $A\beta = 1$, the circuit acts as oscillator

frequency of oscillation $f_0 = \frac{1}{2\pi\sqrt{LC}}$

where $L = L_1 + L_2 + 2M$

M → mutual inductance between coils L_1 & L_2

→ condition for sustained oscillation

$$h_{fe} \geq \frac{L_1 + M}{L_2 + M}$$

Analysis.

$$Z_1 = j\omega L_1 + j\omega M$$

$$Z_2 = j\omega L_2 + j\omega M$$

$$Z_3 = \frac{1}{j\omega C} = \frac{-j}{\omega C}$$

Sub the values in general equation of oscillator

we get

$$j\omega hie\left[L_1+L_2+2M-\frac{1}{\omega^2 C}\right]-\omega^2(L_1+M)\left[(L_2+M)(1+hfe)-\frac{1}{\omega^2 C}\right]=0 \quad \text{——— (1)}$$

freq. f_0 is determined by equating imaginary part to 0

$$\left[L_1+L_2+2M-\frac{1}{\omega^2 C}\right]=0$$

$$L_1+L_2+2M=\frac{1}{\omega_0^2 C}$$

$$\frac{1}{\omega_0^2}=C\left[L_1+L_2+2M\right]$$

$$\omega_0^2=\frac{1}{C\left[L_1+L_2+2M\right]}$$

$$\frac{\omega_0}{2\pi}=\frac{1}{2\pi\sqrt{(L_1+L_2+2M)C}}=f_r \quad \text{— (2)}$$

→ condition for maintenance of oscillation is obtained by Subs. (2) in (1)

imaginary part becomes 0 & hence

$$(L_2+M)(1+h_{fe}) - \frac{1}{\omega_0^2 C} = 0 \quad \text{— (3)}$$

Sub (2) in above equn. we get

$$\therefore \frac{1}{\omega_0^2 C} = (L_2+M)(1+h_{fe})$$

$$L_1+L_2+2M = (L_2+M)(1+h_{fe})$$

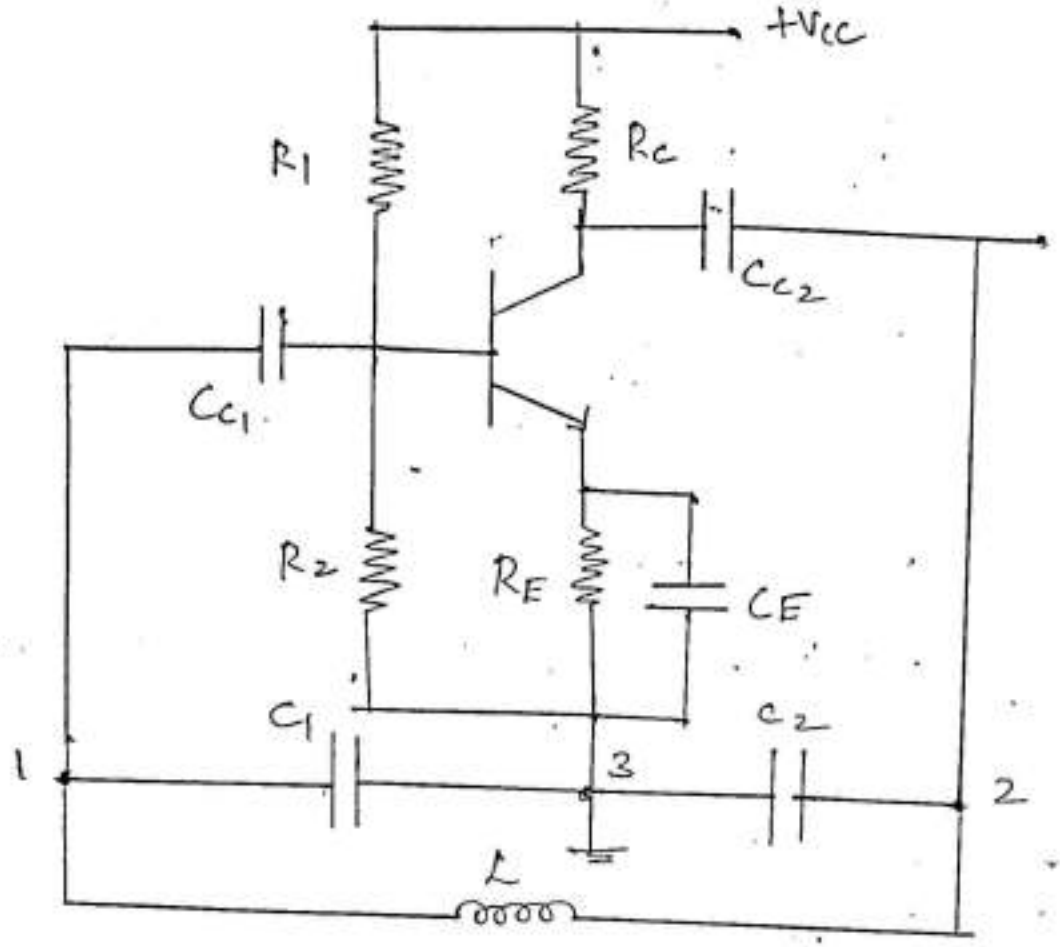
$$L_1+L_2+2M = L_2 + L_2 h_{fe} + M + M h_{fe}$$

$$L_1+L_2+2M - L_2 - M = h_{fe}(L_2+M)$$

$$L_1+M = h_{fe}(L_2+M)$$

$$\boxed{h_{fe} = \frac{L_1+M}{L_2+M}}$$

Collpitts Oscillator



Z_1, Z_2 → are capacitors

Z_3 is inductor

CC_1, CC_2 are coupling capacitors

→ feedback network C_1, C_2, L determines frequency of oscillation

→ when V_{cc} is switched ON, transient current is produced in tank circuit

→ Oscillatory current in tank circuit produces a.c voltages across C_1 & C_2

→ 3 is earth, terminal 1 is positive and terminal 2 is negative

→ Phase difference between 1 & 2 provides 180° and transistor provides 180° phase difference

→ Total phase difference is $180° + 180° = 360°$

→ The necessary condition for sustained oscillation is satisfied

→ The feedback is adjusted so that loop gain

$A\beta = 1$

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

$$\frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2} \qquad \text{(or)} \quad C = \frac{C_1 C_2}{C_1 + C_2}$$

Analysis

$$Z_1 = \frac{1}{jwC_1} = \frac{-j}{wC_1}$$

$$Z_2 = \frac{1}{jwC_2} = \frac{-j}{wC_2}$$

$$Z_3 = jwL$$

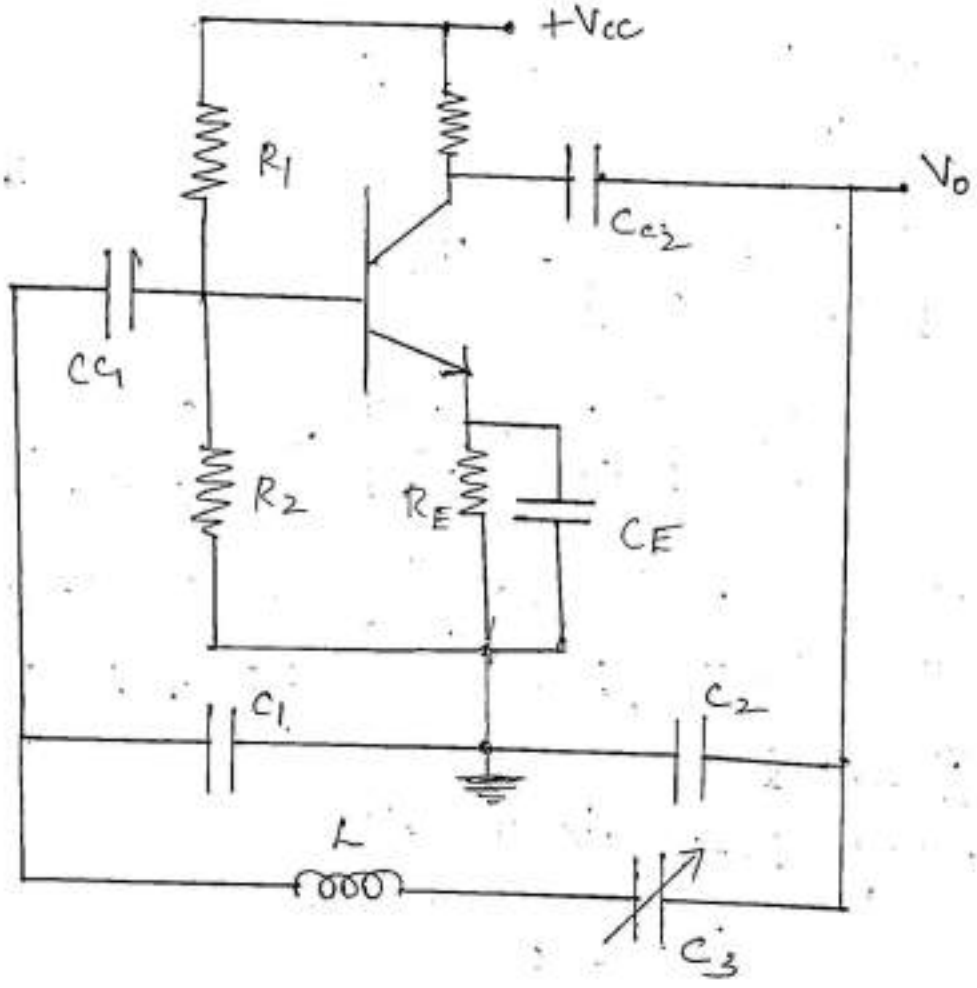
Sub. these in standard equation

$$h_{fe} C_1 = C_2$$

$$h_{fe} = C_2/C_1$$

$$\boxed{h_{fe} = \frac{C_2}{C_1}}$$

clapp oscillator



Z_1 & Z_2 are capacitors

Z_3 is series combination of L and C_3

C_3 improves frequency stability

$$j\,hie\left(\frac{1}{\omega C_1}+\frac{1}{\omega C_2}-\omega L\right)+\left(\frac{1+h_{fe}}{\omega^2 C_1 C_2}-\frac{L}{C_1}\right)=0 \quad -(2)$$

frequency of oscillation, f_o is found by equating imaginary part to 0

$$f_o=\frac{\omega_0}{2\pi}=\frac{1}{2\pi}$$

$$\frac{1}{\omega_0 C_1}+\frac{1}{\omega_0 C_2}-\omega_0 L=0$$

$$\frac{1}{\omega_0}\left[\frac{1}{C_1}+\frac{1}{C_2}\right]=\omega_0 L$$

$$\omega_0^2=\frac{1}{L}\left[\frac{1}{C_1}+\frac{1}{C_2}\right]=\frac{C_2+C_1}{L C_1 C_2}$$

$$f_o=\frac{\omega_0}{2\pi}=\frac{1}{2\pi}\sqrt{\frac{C_2+C_1}{L C_1 C_2}}=\frac{1}{2\pi}\sqrt{\frac{C_2+C_1}{L C_1 C_2}} \quad -(3)$$

Sub (3) in (2)

imaginary part is 0 so

$$\frac{1+h_{fe}}{\omega_0^2 C_1 C_2}-\frac{L}{C_1}=0$$

$$\frac{1+h_{fe}}{\frac{C_2+C_1}{L C_1 C_2}\times C_1 C_2}=\frac{L}{C_1}$$

$$L(1+h_{fe})C_1=L(C_2+C_1)$$

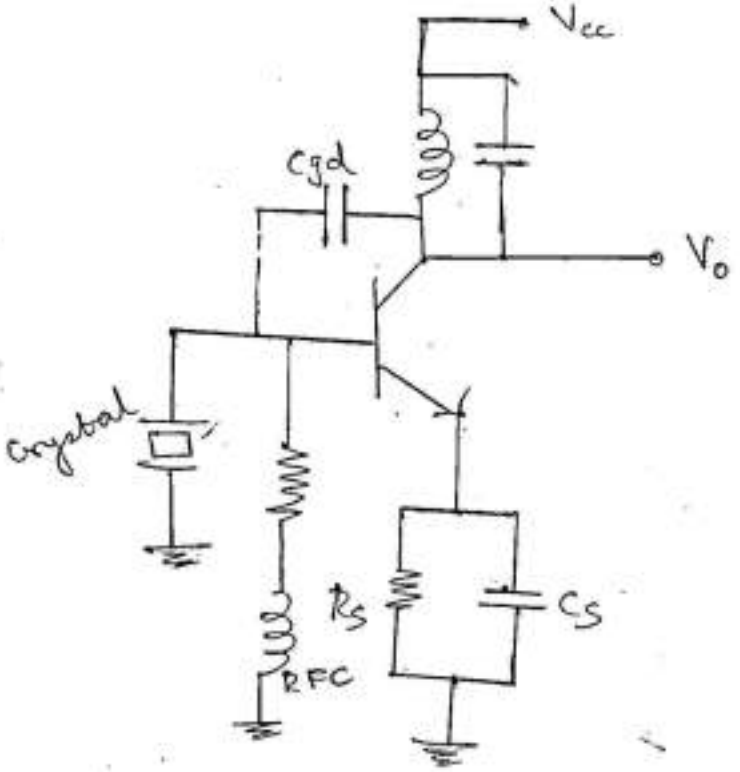
$$C_1+h_{fe}C_1=C_2+C_1$$

Crystal oscillator

→ crystal is thin slice of piezo electric material such as quarty, tourmaline rochelle salt which exhibits piezo electric effect

→ piezo electric effect is that the crystal reacts to any mechanical stress by producing an electric charge in reverse effect. electric field results in mechanical strain

→ high degree of frequency stability is obtained in crystal oscillator



$$\omega L_1 - \frac{1}{\omega C_1} = \frac{1}{\omega C_2} + \frac{1}{\omega C_3}$$

$$\omega L_1 = \frac{1}{\omega C_1} + \frac{1}{\omega C_2} + \frac{1}{\omega C_3}$$

$$\omega^2 L_1 C_1 = 1 + \frac{C_1}{C_2} + \frac{C_1}{C_3}$$

$$f_o = \frac{1}{2\pi\sqrt{L_1 C_1}} \sqrt{1 + \frac{C_1}{C_2} + \frac{C_1}{C_3}}$$

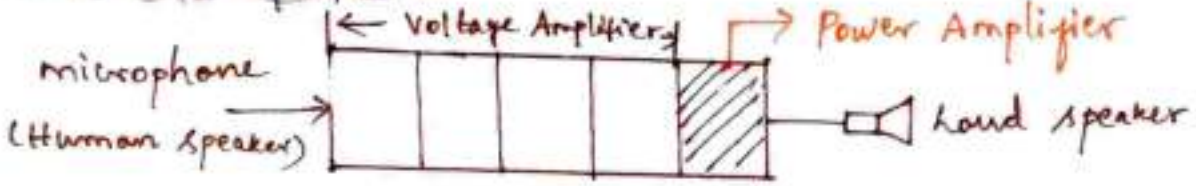
→ It uses a particular combination of an inductor and three capacitors. to set the oscillator frequency

→ the oscillator has positive feedback.

Unit-5

Power Amplifiers and DC convertors

Power Amplifiers



→ In a public address system, there are many stages connected in cascade

→ The input and intermediate stages are small signal amplifiers

→ The last stage gives output to load like loud speaker.

→ A stage which develops sufficient power to the load like loud speaker is called large signal Amplifier or Power Amplifier

Power Amplifiers finds application in public address systems, radio receivers, Industrial control system, tape players, T.V receivers and CRT.

Types

→ the position of Q point on load line decides the class of operation of power amplifier

→ The various classes of power Amplifier are

i) class A ii) class B iii) class C and iv) class AB

class A amplifier

→ In class A amplifier Q point is selected at the centre of load line

→ The output flows for full input cycle

→ The transistor remains in active region for full cycle

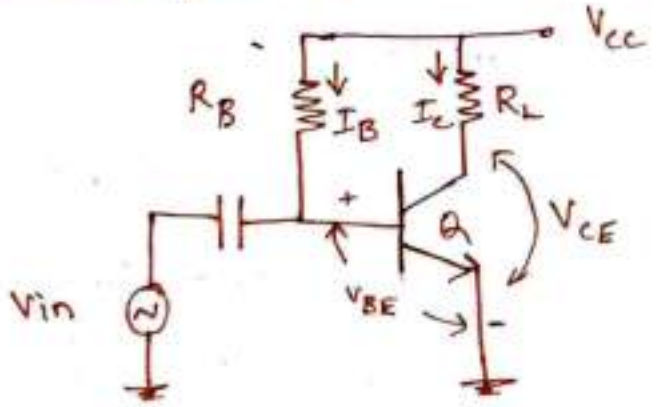
→ The collector current flows for 360°

Types of class A

i) Directly coupled class A amplifier (series fed)

ii) Transformer coupled class A

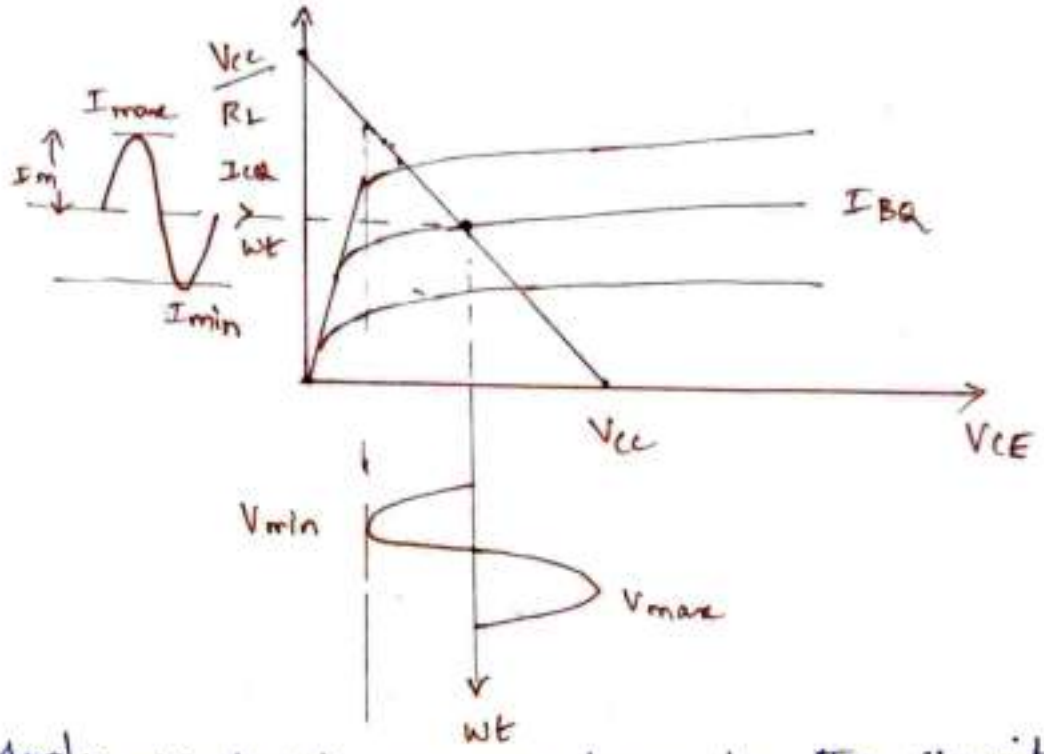
Series fed, Directly coupled class A



→ In directly coupled, the load is directly connected in collector circuit

→ The transistor is used is power transistor

→ The value of R_B is selected such a way that Q pt. lies in centre of d.c load line.



→ Apply Kirchoff's voltage law to the circuit

$$V_{cc} = I_c R_L + V_{CE}$$

$$I_c R_L = -V_{CE} + V_{cc}$$

$$I_c = \left[-\frac{1}{R_L}\right] V_{CE} + \frac{V_{cc}}{R_L}$$

→ The slope of load line is $-\frac{1}{R_L}$ and y interapt is $\frac{V_{cc}}{R_L}$

DC operation

→ The collector supply voltage V_{cc} and resistance R_B devides dc bias current I_{BQ}

→ Applying KVL to base emitter loop

$$I_{BQ} = \frac{V_{cc} - 0.7}{R_B}$$

$$I_{CQ} = \beta I_{BQ}$$

$$V_{CEQ} = V_{cc} - I_{CQ} R_L$$

DC power input

→ DC power input is

$$P_{DC} = V_{cc} \cdot I_{CQ}$$

AC power output

$$V_m = \frac{V_{PP}}{2} = \frac{V_{max} - V_{min}}{2}$$

V_m → amplitude of a.c output voltage

V_{max} → maximum instantaneous value of collector voltage

V_{min} → minimum instantaneous value of collector voltage

V_{PP} → peak to peak value of a.c output voltage

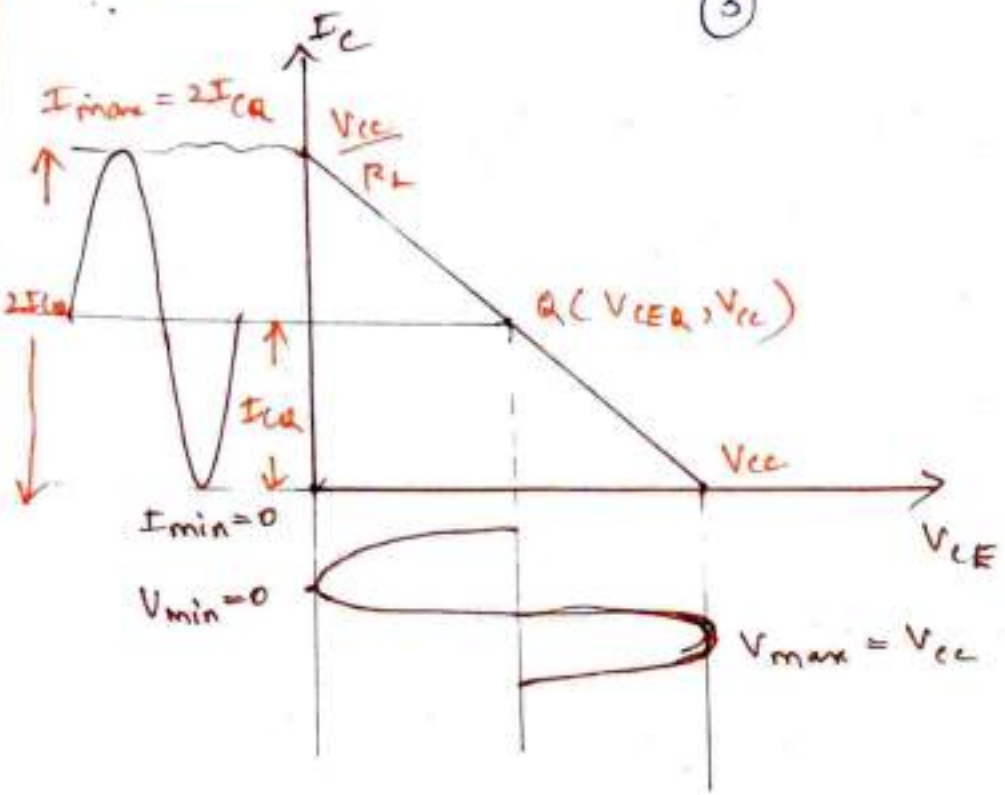
$$P_{ac} = \frac{V_m I_m}{2} \quad \frac{\frac{V_{PP}}{2} \times \frac{I_{PP}}{2}}{2}$$

$$P_{ac} = \frac{V_{PP} \times I_{PP}}{8}$$

$$P_{ac} = \frac{I_{PP}^2 R_L}{8}$$

$$P_{ac} = \frac{V_{PP}^2}{8R_L}$$

$$P_{ac} = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8}$$



$V_{max} = V_{cc}$ & $V_{min} = 0$

$I_{max} = 2I_{CQ}$ & $I_{min} = 0$

$$\%\eta = \frac{(V_{cc}-0)(2I_{CQ}-0)}{8 V_{cc} I_{CQ}} \times 100 = \frac{2 V_{cc} I_{CQ}}{8 V_{cc} I_{CQ}} \times 100$$

$$= 25\%$$

Power Dissipation

$$P_d = P_{DC} - P_{ac}$$

→ maximum power dissipation occurs when there is no a.c input signal

$$P_{d\,max} = V_{cc} \times I_{CQ}$$

Advantages:

→ circuit is simple to design
→ load is connected directly no transformer is necessary
→ less no. of components is required

Disadvantages

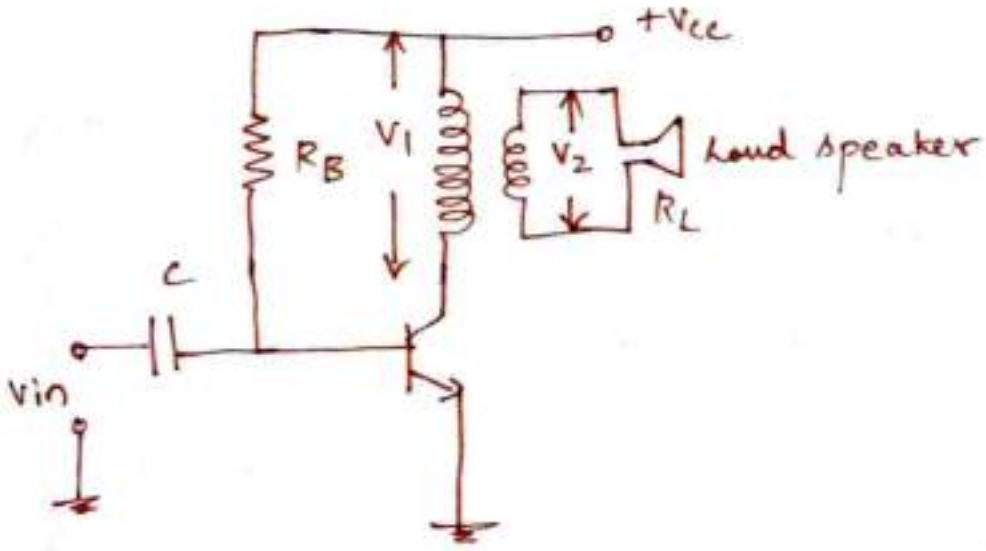
1. Since load resistance is directly connected in collector there is wastage of power
2. Power dissipation is more
3. the output impedance is high
4. The efficiency is very poor.

Transformer coupled class A Amplifier

→ For maximum power transfer to load, impedance matching is necessary

→ the loudspeaker has low output impedance which has to be matched with class A amplifier of high output impedance

→ This is eliminated by using transformer to deliver power to load.



Dc operation

Apply KVL to collector circuit

$$V_{cc} - V_{CE} = 0$$

$$V_{cc} = V_{CE}$$

$$\boxed{V_{CEQ} = V_{cc}}$$

Dc operation power input

$$P_{DC} = V_{cc} I_{CQ}$$

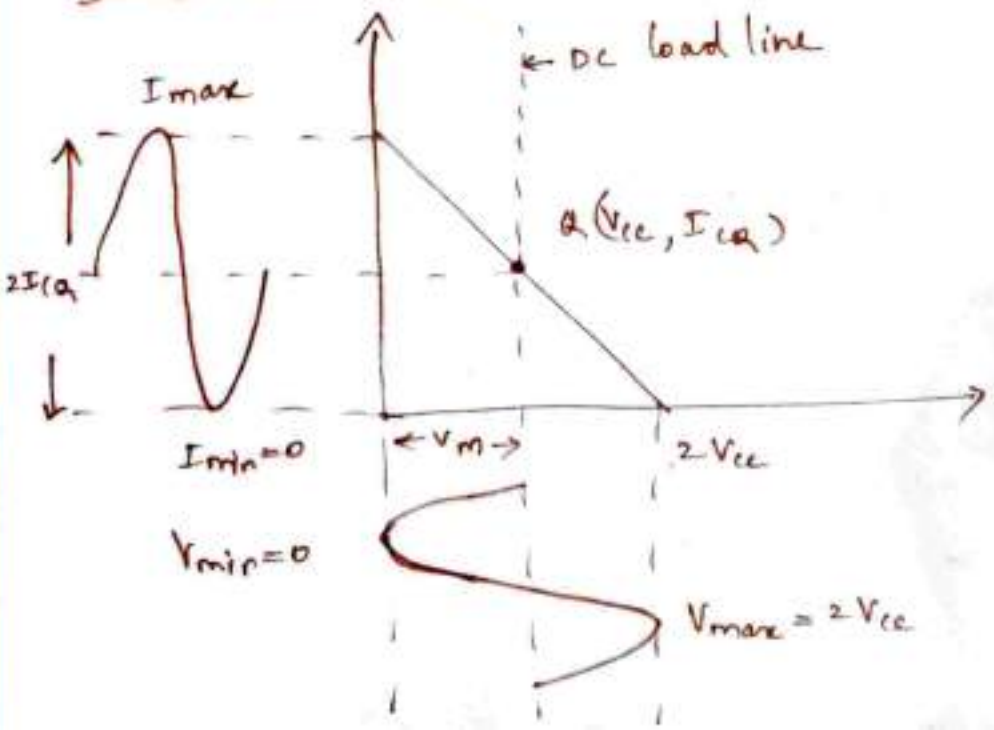
Ac output power

$$P_{ac} = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8}$$

Efficiency

$$\% \eta = \frac{P_{ac}}{P_{dc}} \times 100 = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8 V_{cc} I_{CQ}} \times 100$$

maximum Efficiency



$V_{min} = 0$ and $V_{max} = 2V_{cc}$

$I_{min} = 0$ and $I_{max} = 2I_{CQ}$

$$\% \eta_{max} = \frac{(2V_{cc} - 0)(2I_{CQ} - 0)}{8 V_{cc} I_{CQ}} \times 100$$

$$= \frac{4 V_{cc} I_{CQ}}{8 V_{cc} I_{CQ}} \times 100 = 50\%$$

Power Dissipation

$$P_d = P_{DC} - P_{ac}$$

→ when input signal is larger, more power is delivered to load and less is power dissipation

→ when there is no input signal, the entire dc input power gets dissipated in form of heat

$$P_{d\,max} = V_{cc} \times I_{CQ}$$

Advantages:

1. the efficiency is higher
2. Impedance matching is possible

Disadvantages

1. Due to transformer, the circuit is bulkier
2. The circuit is complicated
3. frequency response is poor.

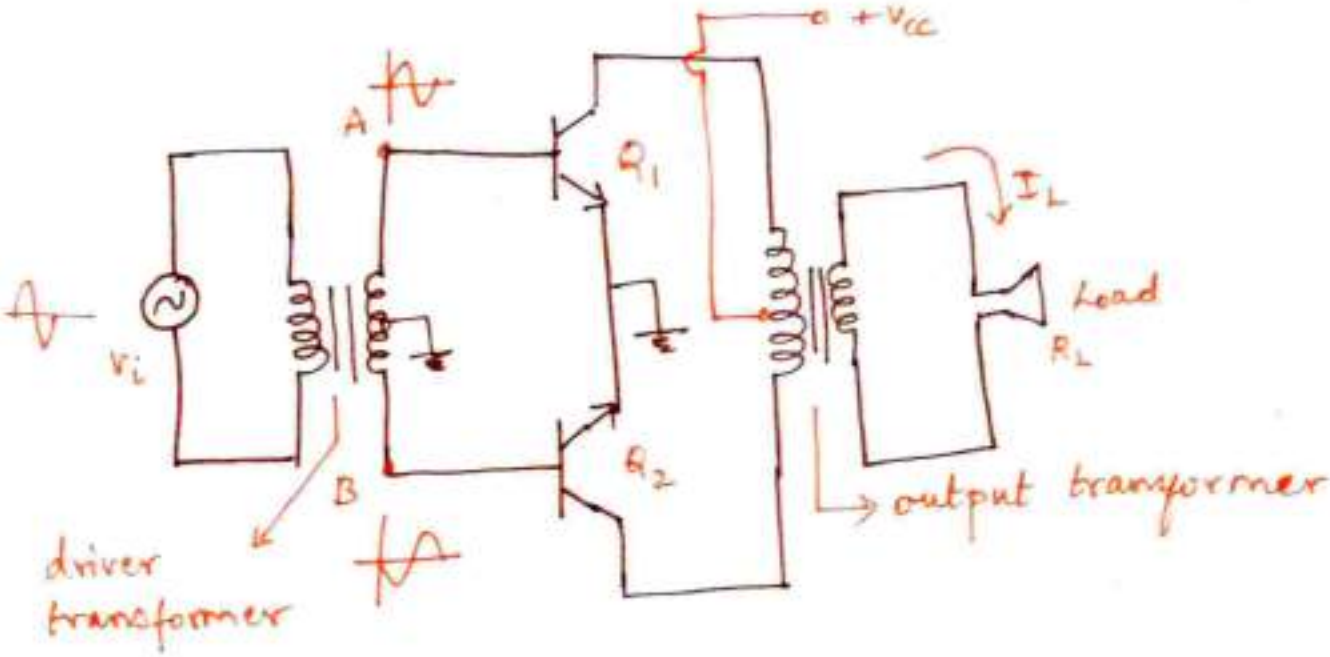
Analysis of class B

→ The Q point is located on x-axis itself.
→ The collector current flows only for half cycle
→ To get full cycle across load, two transistors conduct in alternate half cycle

Two types of class B
1) class B push pull
2) complementary Symmetry class AB

class B push pull

→ It has two transformers, input and output transformer
→ It has two transistors both of same type either npn or pnp.
→ The input signal is applied to primary of driver transformer
→ The centre tap on secondary of driver transformer is grounded
→ The voltage of secondary of driver transformer is equal with opposite polarity
→ The input to base of Q_1 and Q_2 will be 180° out of phase



Operation :

→ for positive half cycle of input A is positive and B is negative

→ Transistor Q_1 conducts and Q_2 is cut off

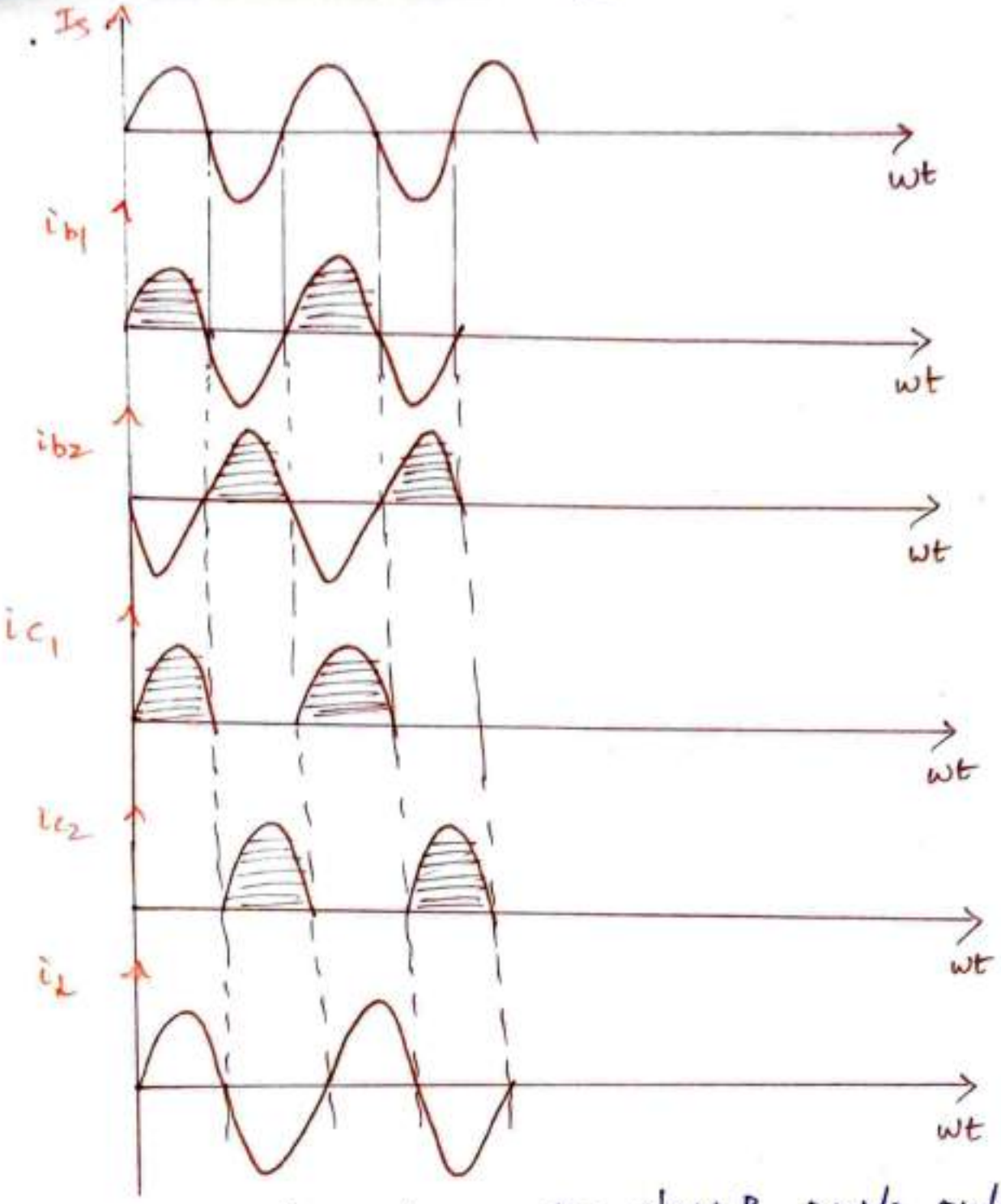
→ So i_{b_1} flows and $i_{b_2} = 0$, and i_{c_1} flows for upper part of primary

→ For negative half cycle, B is positive and A is negative

→ Transistor Q_2 conducts and Q_1 is cutoff.

→ So i_{b_2} flows and $i_{b_1} = 0$, and i_{c_2} flows through lower part of primary

→ Thus full cycle is obtained across the load



Wave form for class B push pull

DC power input

$$P_{dc} = V_{cc} \times I_{dc}$$

$$I_{dc} = \frac{I_m}{\pi} + \frac{I_m}{\pi} = \frac{2I_m}{\pi} \quad (\because \text{two transistor})$$

$$\boxed{P_{dc} = \left(\frac{2I_m}{\pi}\right) \times V_{cc}}$$

Ac power output

$$P_{ac} = \frac{V_m I_m}{2}$$

Efficiency :

$$\% \eta = \frac{P_{ac}}{P_{dc}} \times 100 = \frac{\left(\frac{V_m I_m}{2}\right)}{\frac{2}{\pi} V_{cc} \times I_m} \times 100$$

$$\% \eta = \frac{\pi}{4} \times \frac{V_m}{V_{cc}} \times 100$$

max efficiency :

maximum value of V_m is possible if

$$V_m = V_{cc}$$

$$\% \eta_{max} = \frac{\pi}{4} \times \frac{V_{cc}}{V_{cc}} \times 100 = 78.5\%$$

$$\boxed{\% \eta = 78.5\%}$$

Power dissipation

$V_m = \frac{2}{\pi} V_{cc}$ - for max. power dissipation

$$P_d = P_{dc} - P_{ac} = \frac{4}{\pi^2} \frac{V_{cc}^2}{R_L'} - \frac{2}{\pi^2} \frac{V_{cc}^2}{R_L'}$$

$$P_{d\,max} = \frac{2}{\pi^2} \frac{V_{cc}^2}{R_L'}$$

$$\boxed{P_{d\,max} = \frac{2}{\pi^2} \frac{V_{cc}^2}{R_L'}}$$

Advantages:

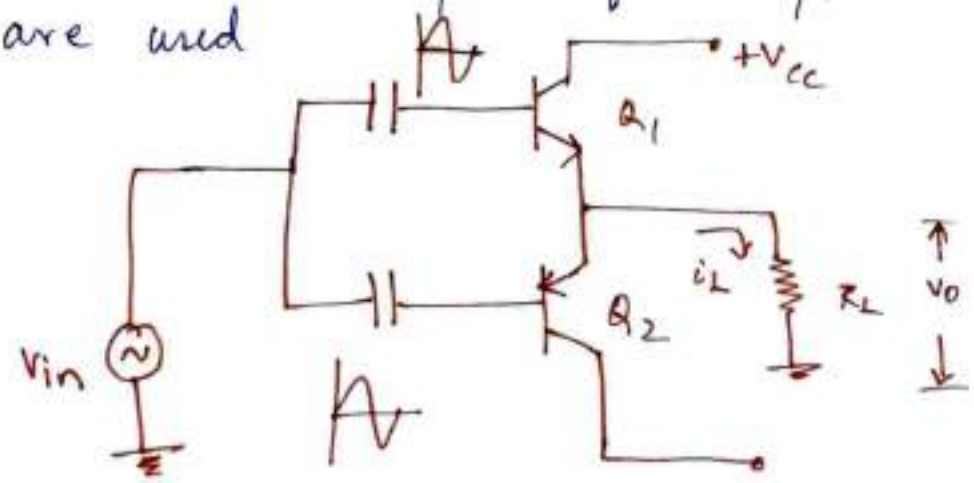
1) Efficiency is much higher than class A
2) Due to transformer impedance matching is possible

Disadv:

1) 2 centre tap transformer are necessary
2) Transformer make the circuit bulky and costlier
3) Frequency response is poor

Complementary symmetry class B Amplifier

→ instead of same type of transistor (npn or pnp) one npn and one pnp is used.
→ so this circuit is transformer less circuit
→ It is diffiudt to match the output impedance
→ Hence matched pair of Complementary transistors are used



→ The circuit is driven from dual supply of $+V_{cc}$

→ Q_1 is npn & Q_2 is pnp

→ During positive half cycle Q_1 is driven to active and Q_2 is cutoff

→ So current flows through R_L

→ During negative half cycle Q_2 conducts and Q_1 is cutoff.

→ Hence Q_2 conducts during negative half cycle of input and current flows thro' R_L.

Analysis is same as class B pushpull

Advantages:

1. As circuit is transformer less, weight, size and cost are less
2. Due to common collector impedance matching is possible

Disadvantage

1. It needs two separate voltage supplies
2. Output is distorted to cross over distortion.

Cross over Distortion

→ For transistors to be in active region the base emitter junction must be forward bias

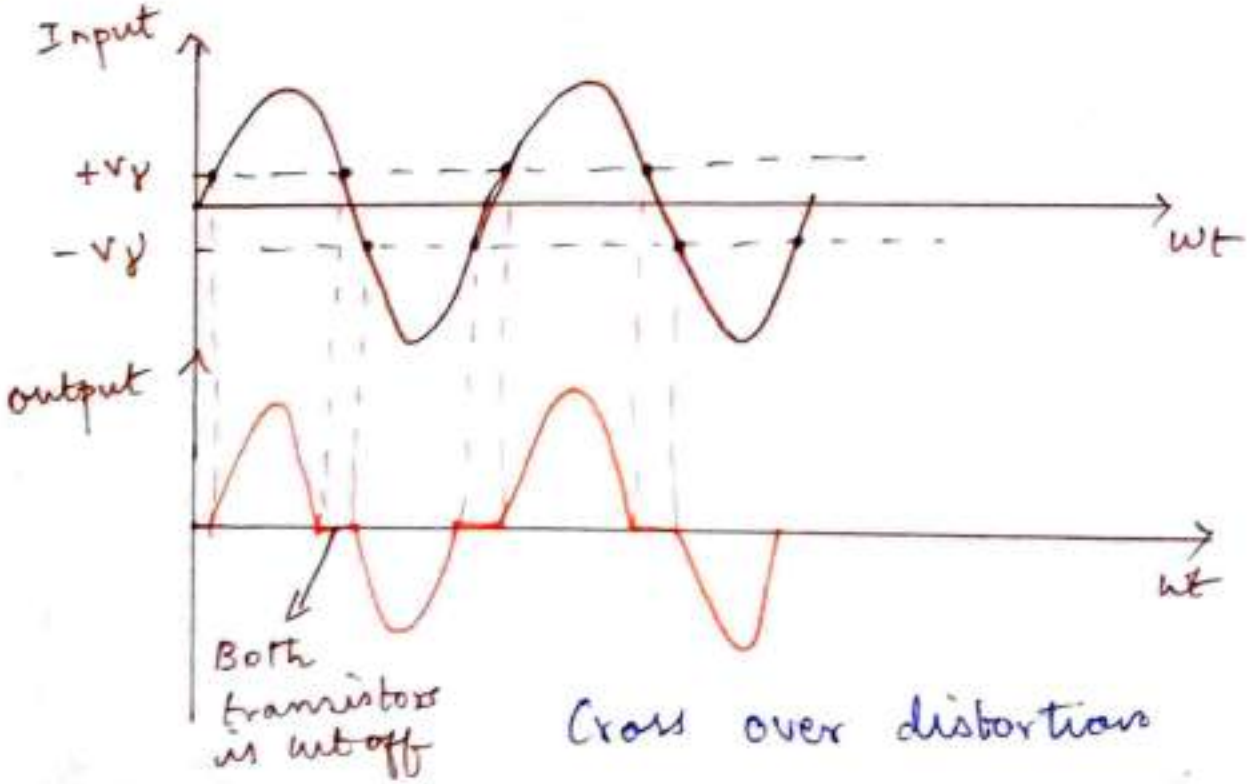
→ the junction is made forward bias till the voltage applied becomes greater than cut in voltage (0.7V) for si

→ when magnitude of input is less than 0.7 the collector current remains zero and transistor remains in cut off.

→ There is a period between crossing of half cycles, none of transistor conducts and output is zero.

→ Hence the nature of output is distorted and do not remains same.

→ Such a distortion is called cross over distortion



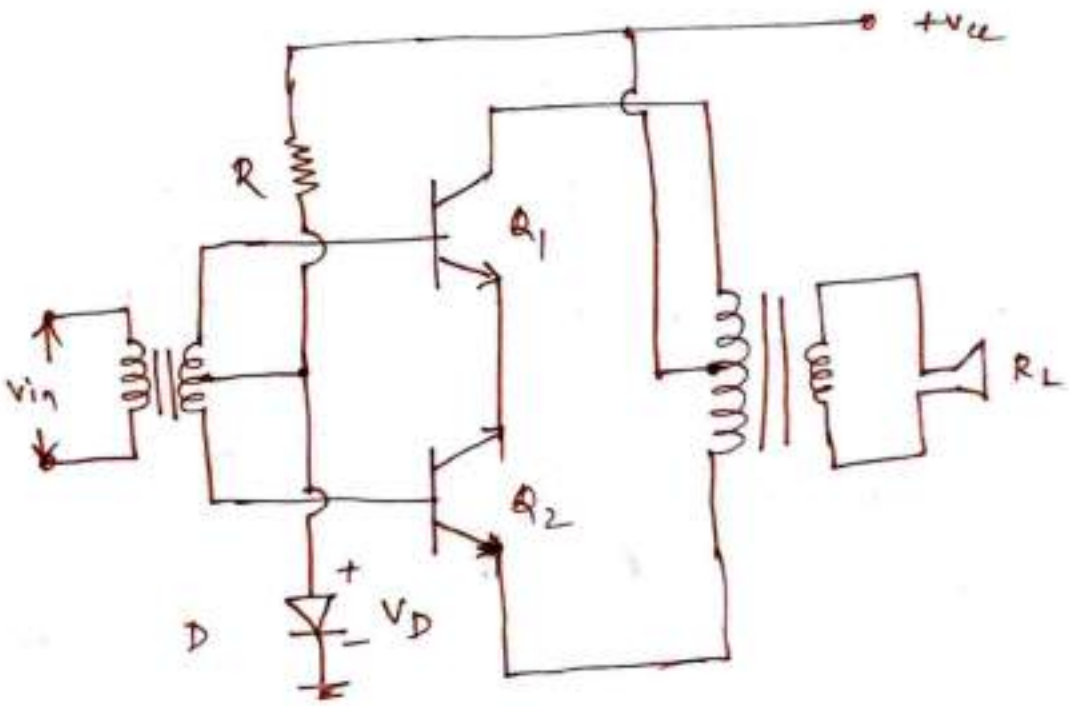
Cross over distortion

Elimination of cross over distortion

To eliminate cross over distortion, a small forward bias is applied to transistor

Push pull class AB

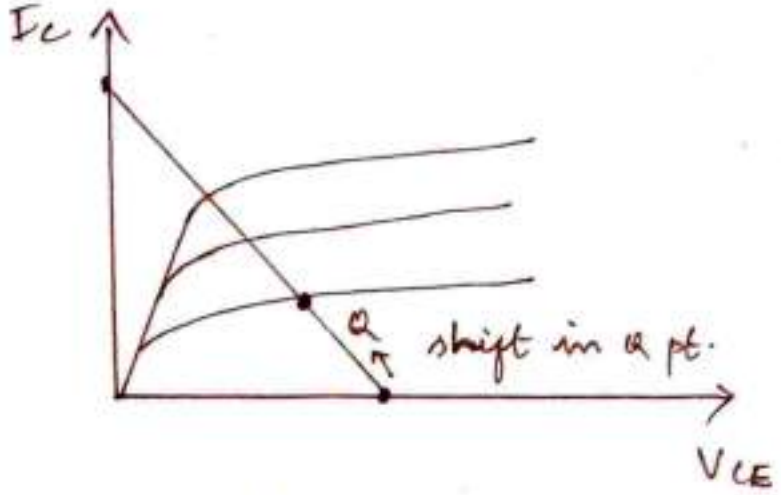
→ The forward bias across the transistor is provided by using diode



→ The drop across diode D is equal to cut in voltage of base emitter junction of transistor

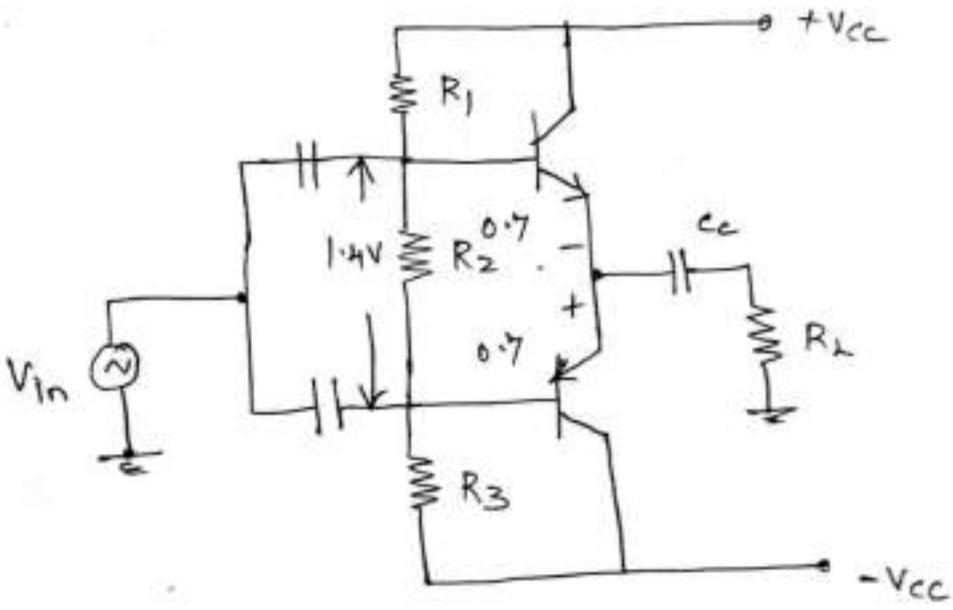
→ Hence both transistor conducts for full cycle

→ The Q point shifts upward and the operation becomes class AB



Complementary Symmetry Class AB

→ In complementary Symmetry, base emitter junction of both Q_1 and Q_2, are required to provide fixed bias



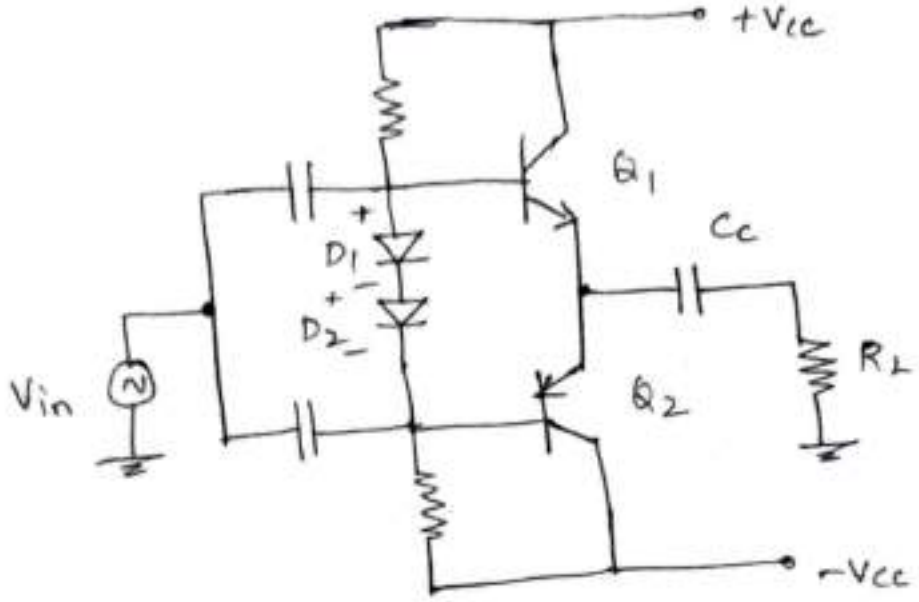
→ For silicon Transistor fixed bias of 0.7+0.7 = 1.4V is required

→ This is achieved by using potential divider arrangement

→ As the junction cut in voltage changes with temperature, there is still possibility of

distortion as temperature changes

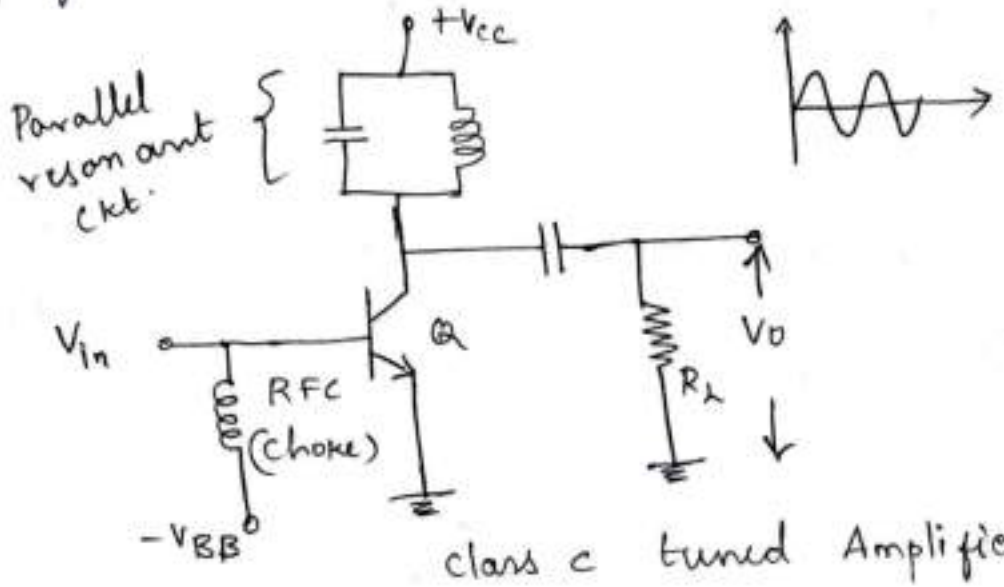
→ Hence instead of R_2, two diodes is used to provide required fixed bias



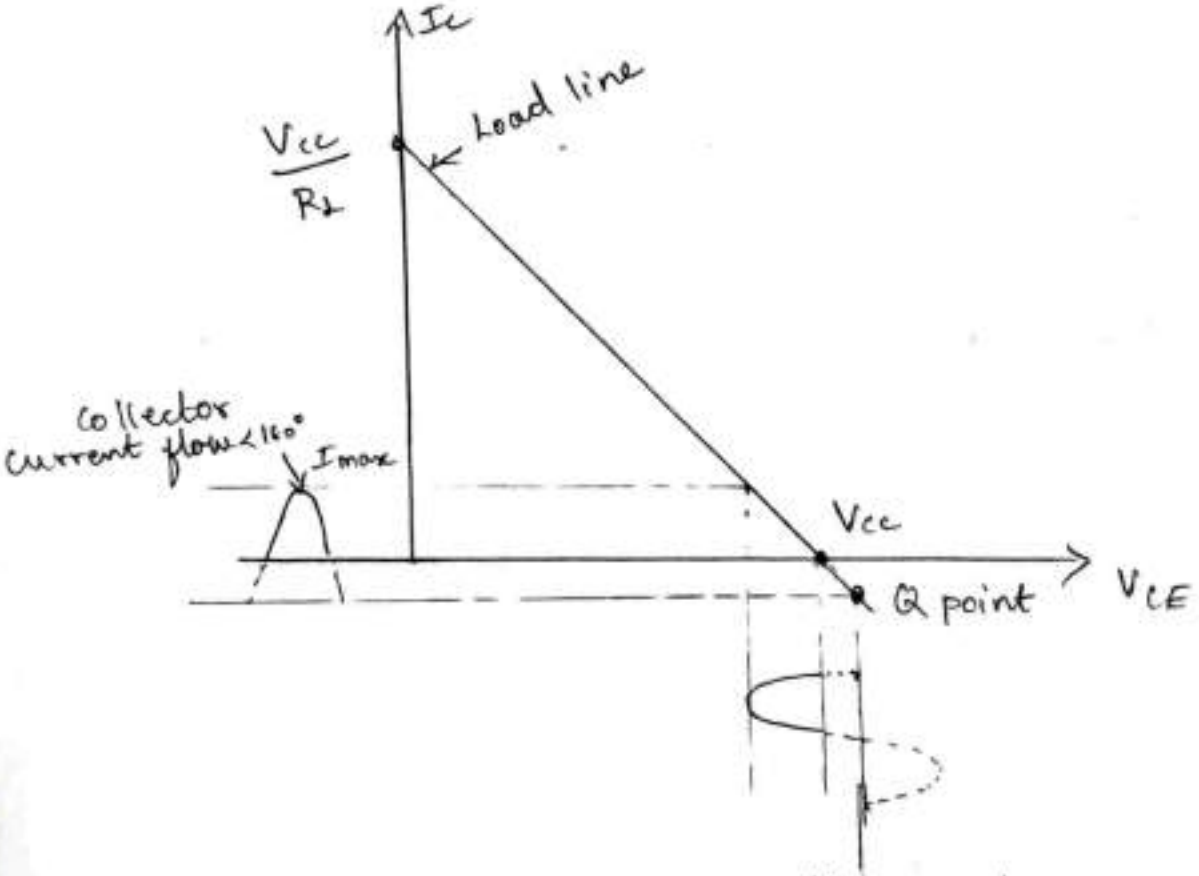
→ As temperature changes along with junction characteristics, the diode get charged and maintain necessary biasing to overcome distortion

Class c operation

→ In class c, resonating circuit is used as load. So most of class c amplifiers are tuned amplifiers



class c tuned Amplifier



waveform representing class c

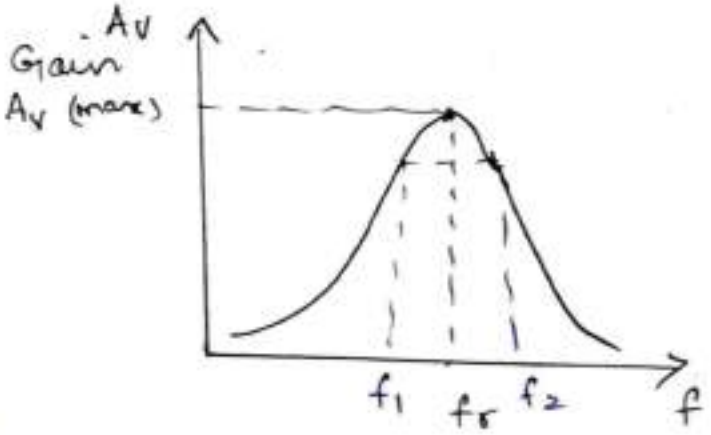
→ A parallel resonant circuit acts as load impedance

→ The collector current flows for less than half a cycle and consists of series of pulses. with harmonics

→ The resonant frequency is given by

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

→ The output Voltage is maximum at resonant frequency. The gain drops on either side



Bandwidth

$$BW = \frac{f_r}{Q}$$

$$B.W = f_2 - f_1$$

Q – Quality factor

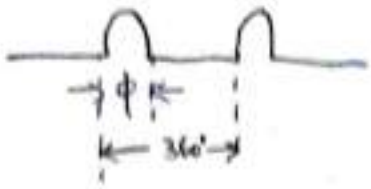
Duty cycle

$$D = \frac{W}{T}$$

W – width of pulse, T – period of pulse

→ Interms of conduction angle

$$D = \frac{\phi}{360^\circ}$$



Output Power

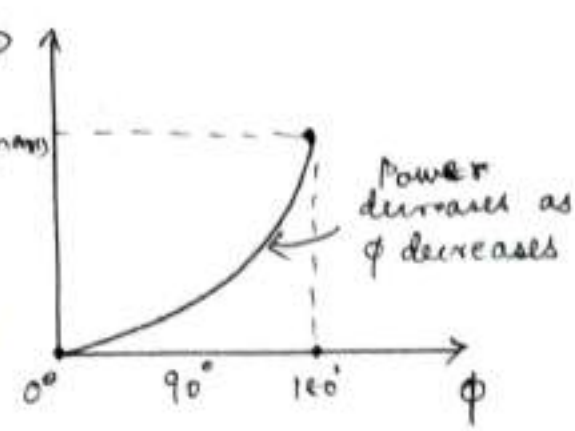
$$P_{out} = \frac{V_{rms}^2}{R_L}$$

$$V_{pp} = 2V_m = 2\sqrt{2}\, V_{rms}$$

$$P_{out} = \frac{(V_{pp}/2\sqrt{2})^2}{R_L} = \frac{V_{pp}^2}{8R_L}$$

Transistor Dissipation

$$P_{D(max)} = \frac{V_{pp\,max}^2}{40\,r_c}$$

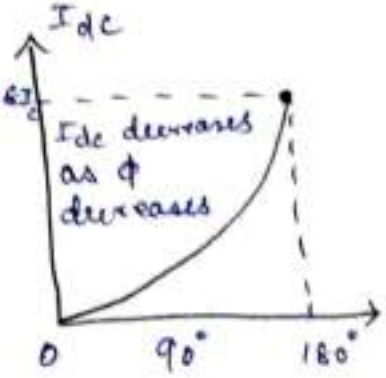


→ Power dissipation depends on conduction angle ϕ

→ less ϕ, less dc power, and less is transistor dissipation

DC Input Power

$$I_{dc} = \frac{I_{c(sat)}}{\pi} = 0.318\, I_{c(sat)}$$



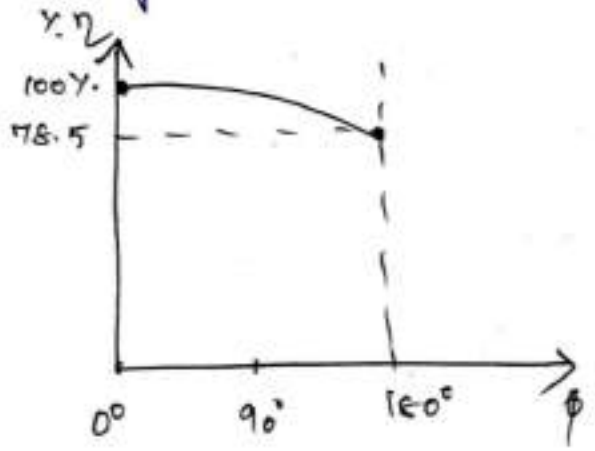
→ If conduction angle is 180°, current is half wave of rectified waveform

Efficiency

→ efficiency is given by ratio of a.c power output to dc power input

$$\%\eta = \frac{P_{out}}{P_{DC}} \times 100 = \frac{P_{out}}{V_{cc} \times I_{dc}} \times 100$$

100% is efficiency is achieved at very small conduction angle



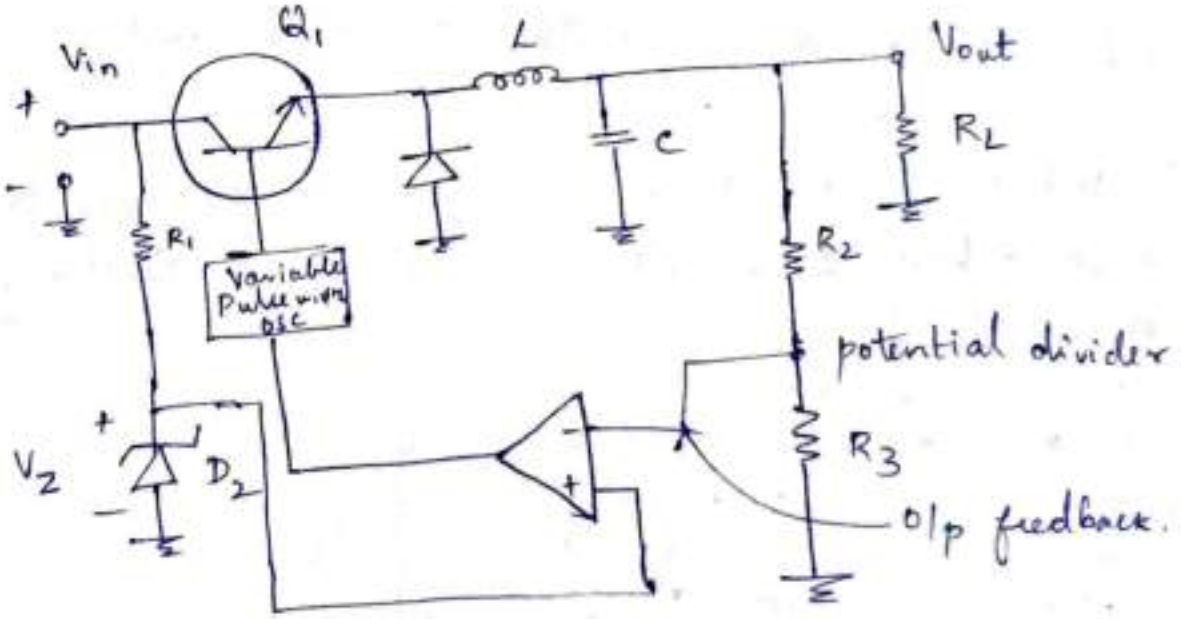
DC/Dc convertors

→ The switch mode regulator is used to describe a ckt which takes dc i/p & provides single d.c o/p

There are three basic configuration of switching regulator

1. Step down or Buck switching regulator
2. Step up or Boost switching regulator
3. Inverting type (Buck-Boost switching regulator)

Step down Switching Regulator (Buck)



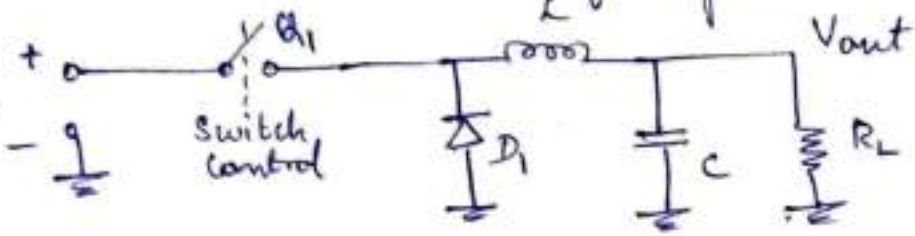
→ It uses an inductor L and series transistor Q_1 which acts as a switch

→ The reference for error amplifier it provided by zener voltage V_Z.

→ The o/p is fed back to error amplifier through potential divider

→ The pulse width oscillator controls the operation of Q_1 as on or off, depending on load requirements

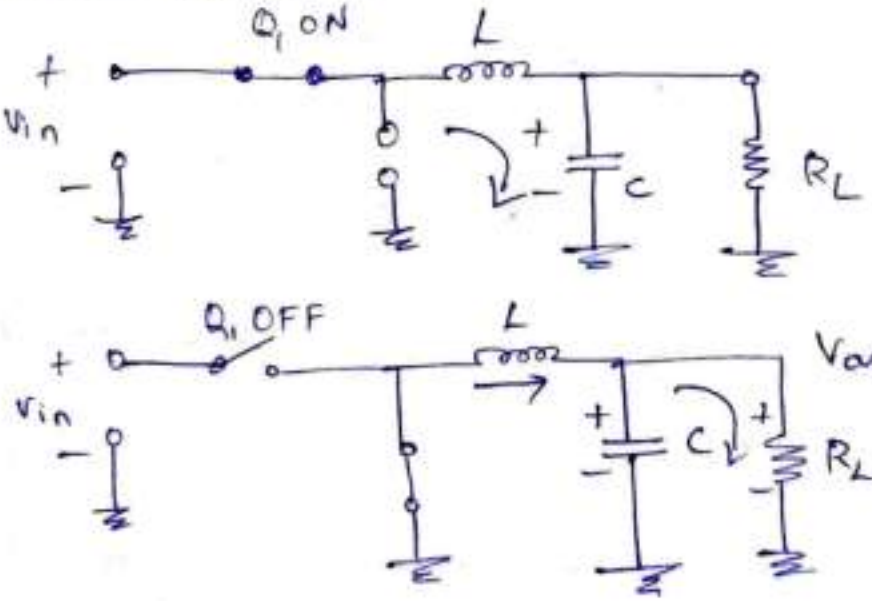
→ The equivalent ckt. of regulator is shown in fig.



→ Q_1 is used for switching the i/p voltage for the required period of time

→ LC filter averages the switched voltage

→ when Q_1 is ON, the capacitor charges thro' it and when Q_1 is OFF, the capacitor discharges thro' load



→ The Variable pulse width oscillator controls ON/OFF periods of Q_1

→ when ON time is more than OFF time, the capacitor charges more, increasing o/p voltage.

→ when OFF time is more, than ON time, the capacitor discharges more, reducing o/p voltage.

→ By adjusting duty cycle $\delta = \frac{t_{on}}{t_{on} + t_{off}}$ of Q_1, the o/p voltage can be regulated

→ If o/p volt ↓, the voltage across R_3 ↓, the error across error amplifier is more

→ this produces pulse of higher width. This increases the charging of capacitor, producing more o/p voltage, Thus the decreased voltage gets compensated

→ If o/p volt ↑, the voltage across R_3 ↑, which produces pulse of smaller width, which reduces t_{on} for Q_1

→ This makes the capacitor to discharge more which increases the o/p voltage

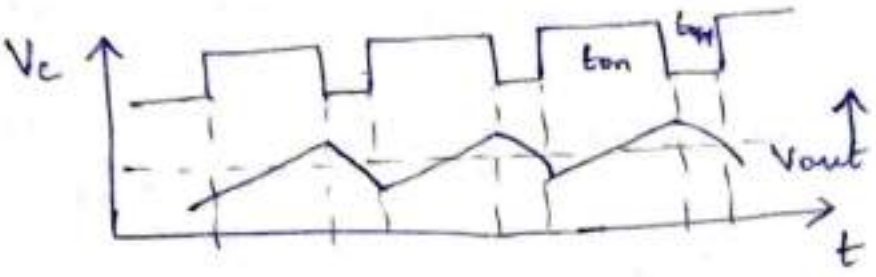
→ Thus o/p voltage is maintained constant by controlling duty cycle of Q_1

→ the o/p voltage is given by

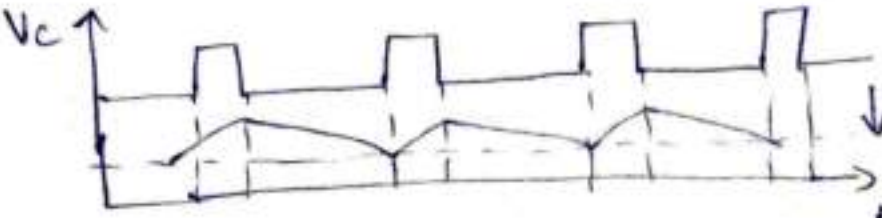
$$\boxed{V_{out} = \delta V_{in}}$$

where $\delta = \frac{t_{on}}{t_{on} + t_{off}} = \frac{t_{on}}{T} = t_{on}(f)$

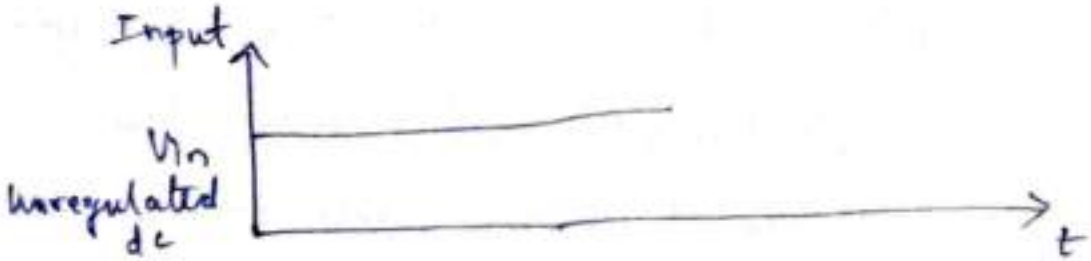
f = frequency

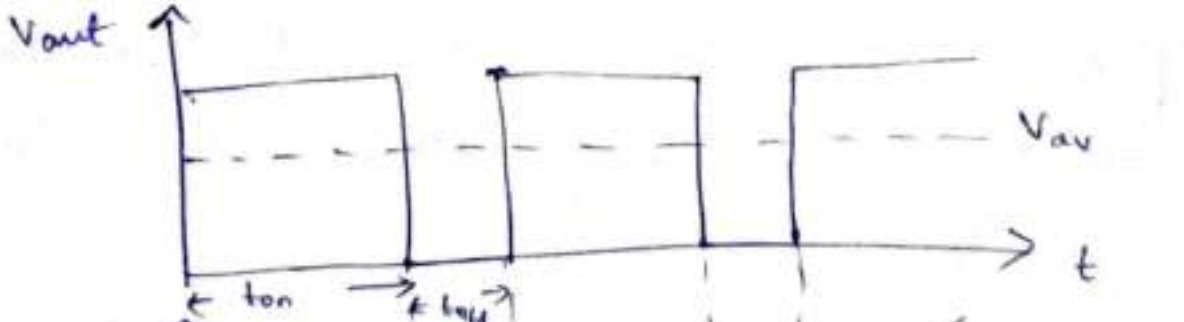


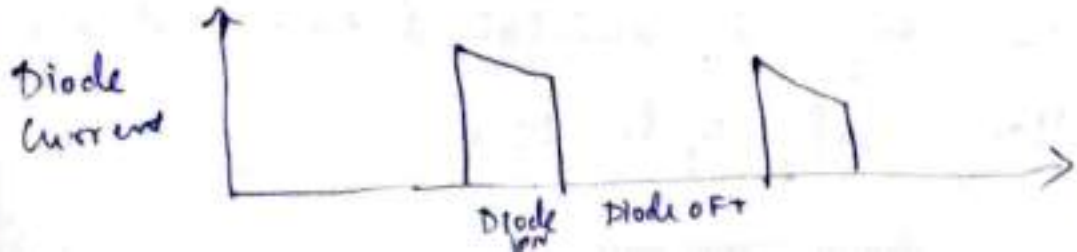
a) $t_{on} > t_{off}$



b) $t_{on} < t_{off}$







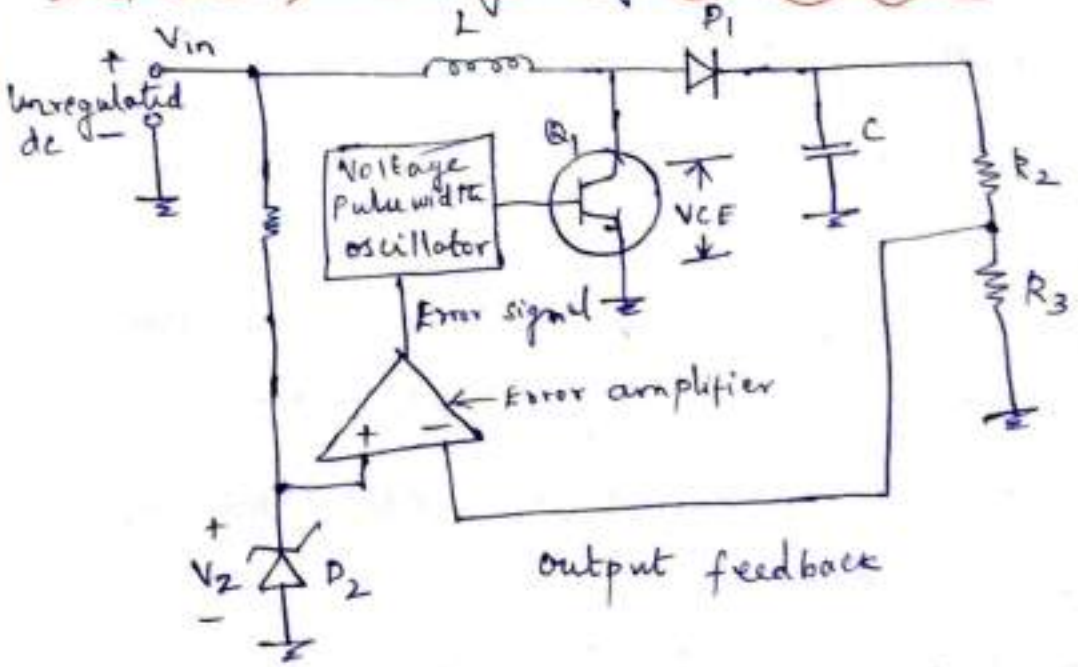
Advantage:

1. High efficiency
2. Simple to design
3. Low ripple content
4. Small output filter.

Disadvantage:

1. Single o/p
2. High i/p ripple
3. No Isolation b/w i/p & o/p
4. Slow transient response

Step Up Switching Regulator (Boost)



→ In Q_1 acts as ON/OFF switch

→ when Q_1 is driven into saturation, V_{CE} is very very small and acts as short circuit.

$V_{in} - V_{CE(sat)}$

Case (1): Let Q_1 is ON (saturation)

→ when Q_1 is ON, V_{CE} is denoted as $V_{CE}(sat)$

→ The voltage across L becomes $[V_{in} - V_{CE(sat)}]$
this expands the magnetic field around the inductor

→ During ON time of Q_1, the voltage across the inductor starts decreasing exponentially from $[V_{in} - V_{CE(sat)}]$

Case :2 Let Q is OFF (cutoff)

→ when Q_1 is OFF, the magnetic field of inductor L, collapses and its polarity gets reversed, since inductor current cannot change instantly.

→ The shorter the ON period, the greater is V_1.

→ The longer the ON time, the smaller the inductor voltage V_1 & less voltage get added to V_{in}, decreasing o/p voltage.

→ when o/p voltage decrease due to increase in load current Then ON time of Q_1 gets reduced

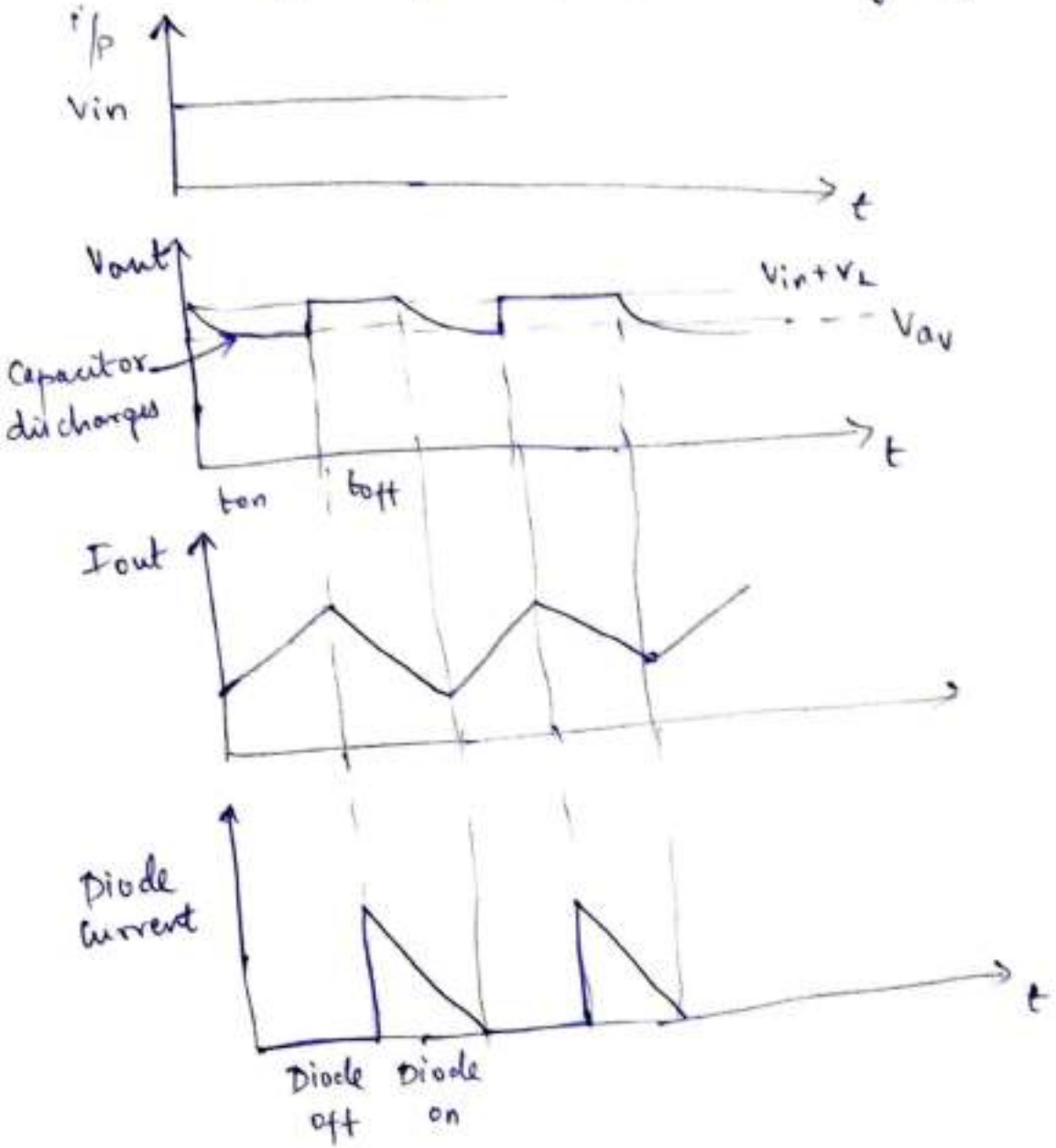
→ when o/p voltage increase, the ON time of Q_1 gets increased.

the output voltage is given by

$$V_{out} = \frac{V_m}{\delta}$$

$$\delta = \frac{t_{on}}{T}.$$

Waveform for step up switching regulator



Advantage

1. o/p voltage is higher than i/p voltage
2. η is high
3. Low i/p ripple
4. Simple in design

Disadvantage:

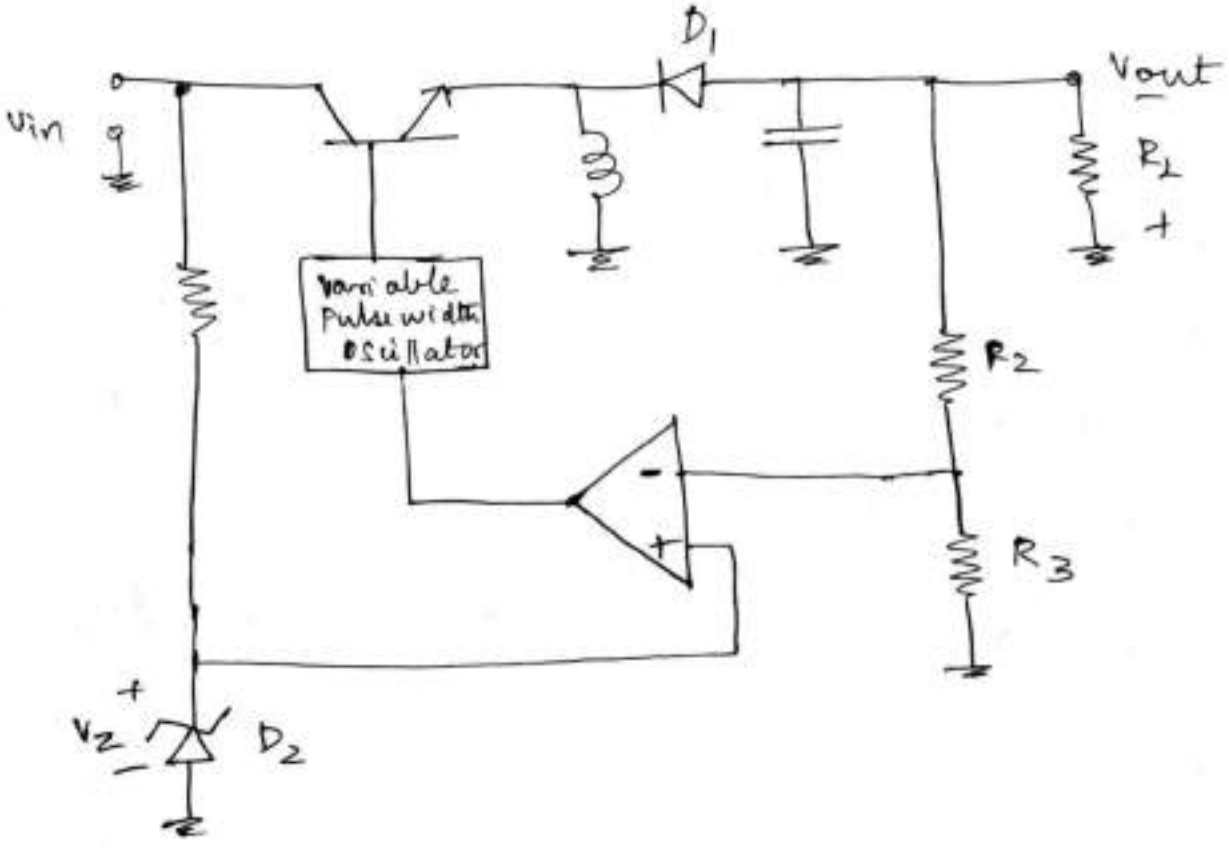
1. It provides single o/p
2. Duty cycle limited to 50%.
3. No isolation b/w i/p & o/p.

Buck-Boost or Voltage Inverter Type Switching Regulator

→ It produces output voltage having polarity opposite to that of input voltage

→ Any change in output produces error which gets amplified by op amp error amplifier

→ this control on/off period of Q_1 to regulate the output, through variable pulse width oscillator



Case: 1 Let Q_1 is switched ON

→ Q_1 goes into saturation and Voltage across it drops to $V_{CE(sat)}$ about 0.3V

→ Due to this voltage across inductor

suddenly rises to $[V_{in} - V_{CE(sat)}]$ and magnetic field around it suddenly expands

→ the inductor value starts exponentially decreasing from initial value $[V_{in} - V_{CE(sat)}]$

Case 2 : let Q_1 is OFF

→ As Q_1 OFF, the magnetic field across L gets collapsed

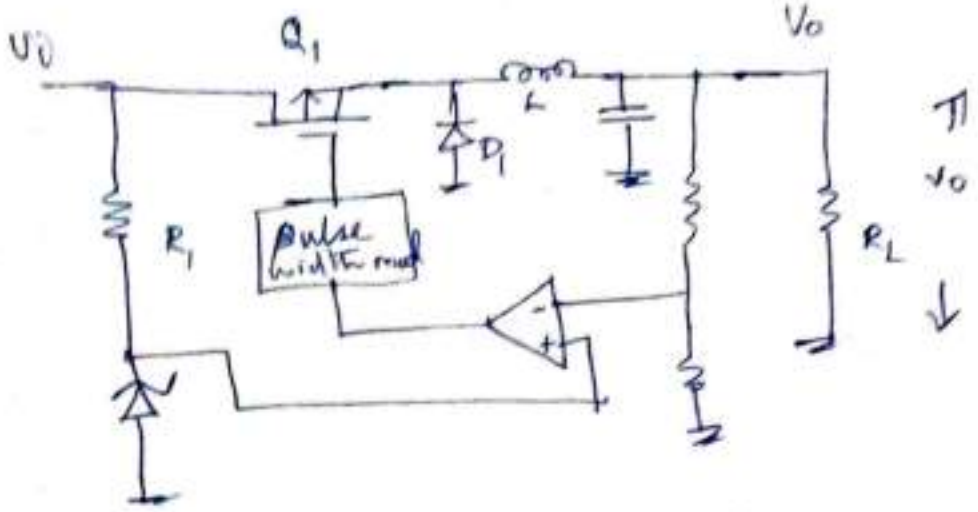
→ Voltage reverses its polarity

→ Due to reverse V_1, diode D_1 is now forward biased

→ The capacitor charges through D_1 producing output voltage of opposite polarity to that of Vin

→ Hence regulator is voltage inverter type

SMPS (MOSFET)



→ when switch is on close

- $V_L = V_i - V_o$ & $V_D = V_L$

→ inductor current will rise

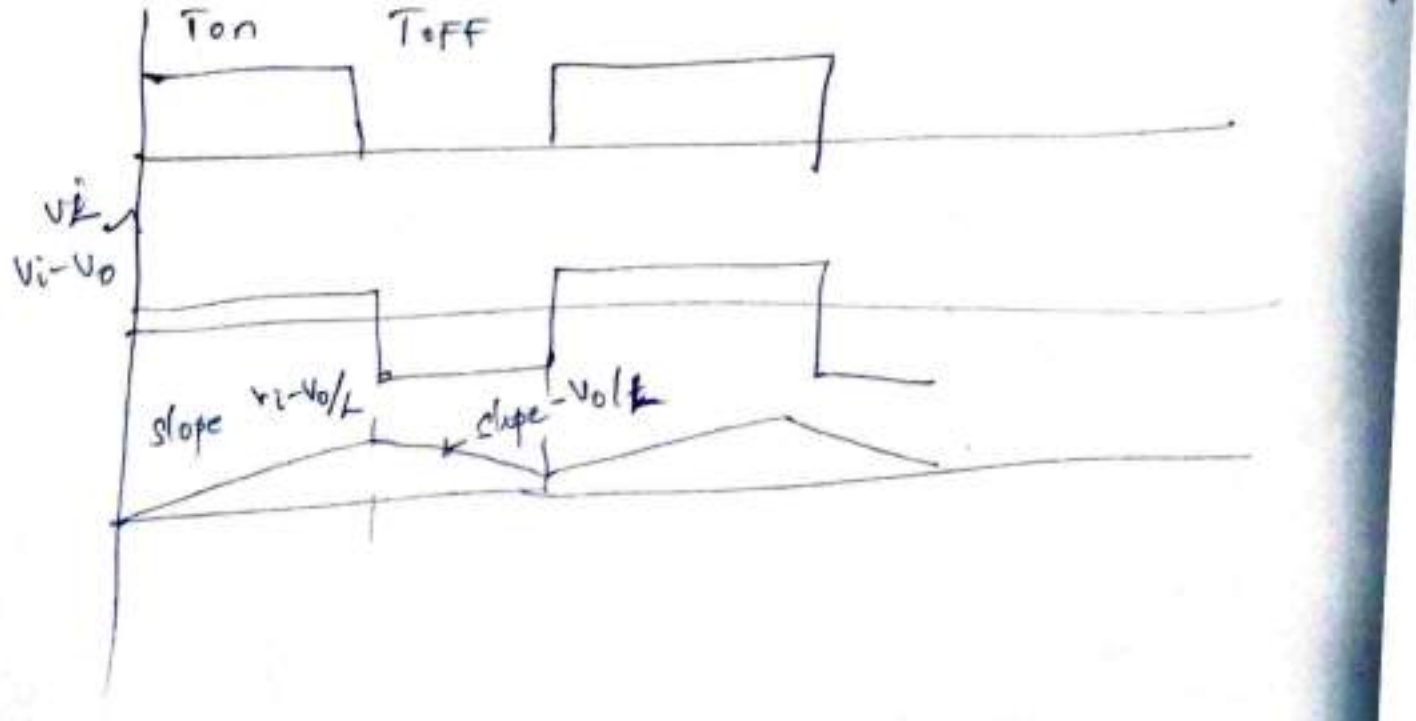
→ Diode D is reverse bias & does not conduct

→ when switch is off current still flows in inductor and into load

$V_L = -V_o$ & $V_D = 0.7$

→ inductor current decreases at rate of $-V_o/L$

→ Diode D is forward biased and conducts $I_L = I_{diode}$



→ R_2/R_1+R_2 is fed back to inverting input of error amplifier

→ difference is given to comparator inverting terminal

→ oscillator generates triangular waveform at fixed freq.

→ o/p of comparator is high when triangular waveform is above the level of error amplifier o/p.

→ when Q_1 is on entire input appears at point A

→ when Q_1 is off, L_1 → supply current to load

→ the diode provides return path for current

→ capacitor C_1 smooths out the voltage at o/p.

$$V_o = \frac{t_{on}}{T} \times V_{in} = \delta V_{in}$$

→ low switch freq improve efficiency and reduce noise but require filtering

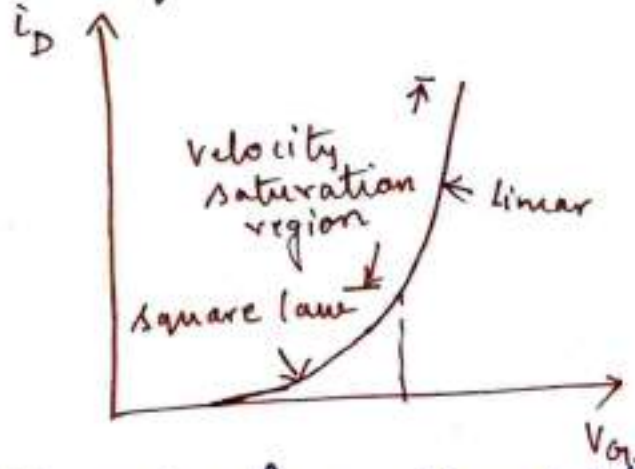
Power MOSFET

→ The operation of power MOSFET is same as conventional MOSFET but power handling of conventional MOSFET is less than 1W.

Features of Power MOSFET

1. Power handling is more than 100W
2. Current handling is in ampere range
3. Large forward conductance
4. As input impedance is very high, large currents can be switched with very small control currents.

characteristics of Power MOSFET



→ power MOSFET have threshold voltages in range of 2V to 4V.

→ In saturation the drain current is related to V_{GS} by square law characteristics

→ The linear portion of characteristics is as a

result of high electric field along short channel causing velocity to reach upper limit, known as velocity saturation.

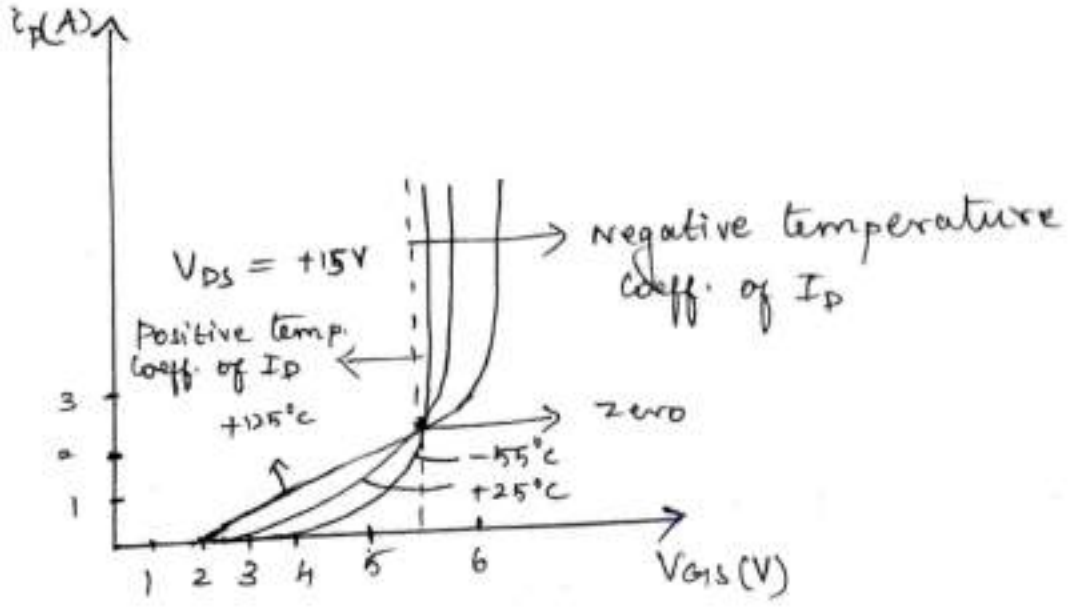
→ The linear i_D-V_{GS} relation implies constant g_m

→ MOSFET is driven in cutoff by applying $V_{GS} < V_{GS(th)}$

→ In ohmic region, MOSFET conducts heavily.

→ In power applications, MOSFET is never operated in active region

MOSFET Temperature effects



→ It is observed that there is value of V_{GS} in the range of 4V to 6V at which temp coeff of i_D is zero

→ At higher values of V_{GS}, i_D exhibits negative temperature coefficient

→ At i_D lower than zero temperature coeff, the temperature coefficient of i_D is positive and MOSFET suffer from thermal runaway

→ the reason for positive temperature coeff. of i_D at low current is that $V_{OV} = V_{GS} - V_t$ is relatively low

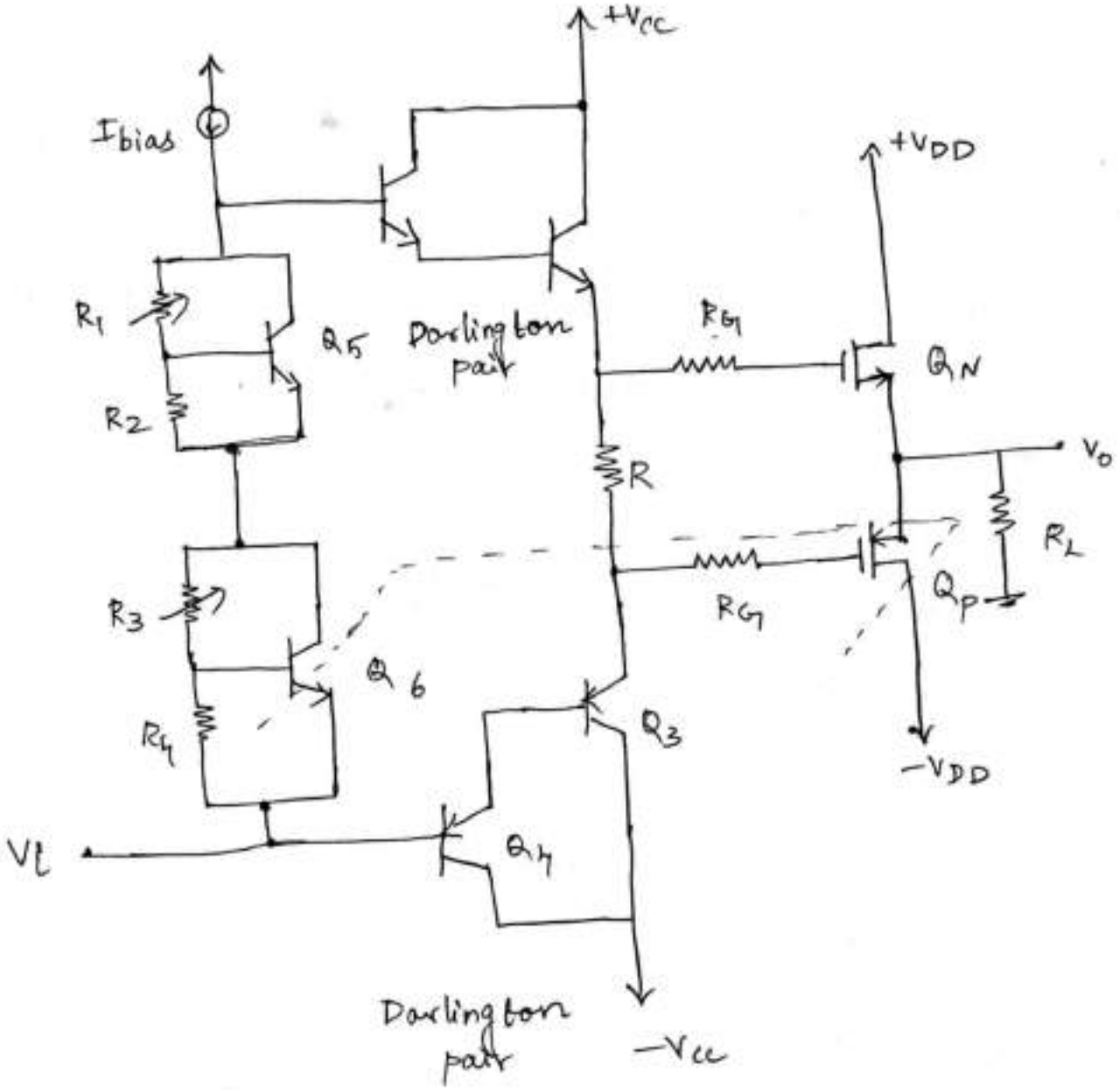
→ Temperature dependence is dominated by negative temperature coefficient of V_t which causes V_{OV} to rise with temperature

class AB power amplifier using power MOSFET

→ The output stage of class AB has a pair of complementary MOSFET

→ BJT are used for biasing and as a driver

→ Complementary Darlington emitter follower formed by Q_1 through Q_4 provide low output resistance necessary for driving output MOSFET at high speeds



class AB push pull amplifier output stage

⇒ The bias circuit uses two V_{BE} multipliers formed by Q_5 and Q_6

→ By adjusting the V_{BE} multiplication factor of Q_6 the bias voltage V_{GG} can be made to decrease with temperature at same rate

$$\star \quad V_{GG} = \left(1+\frac{R_3}{R_4}\right) V_{BE_6} + \left(1+\frac{R_1}{R_2}\right) V_{BE_5} - 4V_{BE}$$

The value of V_{GG} is adjusted to get the desired Q point.